1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DESIGN: X502/MLB_CATZ

LAST CHANGE: Tue Aug 9 17:02:57 2016

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
1	0006782329	ENGINEERING RELEASED	2016-08-10

LAST_MODIFICATION=Tue Aug 9 17:03:06 2016

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49	63	JACK CODEC	AHAAGE	09/22/2015
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52	69	DC-IN & BATTERY CONNECTORS		
53	70	PBUS Supply & Battery Charger		
54	71	VReg CPU VCC Cntl		
55	72	CPU IMVP VCC & VCCSA		
56	73	IMVP VCCSA		
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59	77	VR - OPC (EDRAM)		
60	78	PMIC IC & Power Control		
61	79	PMIC VCCPCH VCCIO 1.8V		
62	80	PMIC 1.2V 1.0V 0.6V		
63	81	RAIL DESENSE CAPS		
64	82	Power FETs		
65	84	LCD Backlight Driver		
66	85	eDP Display Connector	X362	06/23/2015
67	86	SSD MODULE	PAULM	06/15/2015
68	99	DEVELOPMENT ONLY	PAULM	06/15/2015
69	100	Power Aliases	X502-EXP	12/03/2015
70	102	NC_ AND NO_TEST SIGNALS	PAULM	06/15/2015
71	103	Memory Signal Swaps	X502-EXP	12/03/2015
72	104	FCT, ICT PROPERTIES	PAULM	06/15/2015
73	500	=LAST SCHEMATIC PAGE=	MICHKLEE	06/23/2015

DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02265	1	SCHEM,MLB_CATZ,X502	SCH		
820-00875	1	PCBF,MLB_CATZ,X502	MLB	CRITICAL	
639-03266		PCBA,MLB_CATZ,XXXXX,X502			
685-00125	1	COMMON PARTS,MLB_CATZ,X502	CBOM		CMN_PARTS_BOM
985-00239	1	DEV PARTS,MLB_CATZ,X502	DEV1		DEVELOPMENT_LIST

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BOM_COST_GROUP=NO COST ITEMS

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Major ICs

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-00235	1	IC,CPU,SKL-ULT,2+3E,42X24MM,BGA1356	U0500	CRITICAL	CPU_SKL:BASE
998-04195	1	INTERPOSER,VTT ADAPTER,SKL-U,BGA1356	U0500	CRITICAL	CPU_SKL:VTT_INTERPOSER
337S00168	1	CPU,SKYU,QJ8N,D0,QS,2/2,2.3,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.3
337S00170	1	CPU,SKYU,QJ8K,D0,QS,2/2,2.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.6
337S00149	1	CPU,SKYU,QJ57,J0,ES0,2/3,1.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_GD
337S00150	1	CPU,SKYU,QJ58,J0,ES0,2/3,1.6,28W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_BT
337S00219	1	CPU,SKYU,QK2T,K1,SQS,1.8,15W,.95,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_1G8
337S00220	1	CPU,SKYU,QKBY,K1,SQS,2.2,15W,1.05,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G2
337S00222	1	CPU,SKYU,QK33,K1,SQS,2.0,15W,1.0,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G0
337S00233	1	CPU,SKYU,QK32,K1,SQS,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G4
337S00232	1	CPU,SKY,SR2JC,K1,PRQ,1.8,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_1G8
337S00239	1	CPU,SKY,SR2JM,K1,PRQ,2.0,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G0
337S00234	1	CPU,SKYU,SR2JL,K1,PRQ,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G4

ACE

353S00422	2	IC,CD3215,USB PWR SWITCH,A0,6X6MM,BGA96	U3100,U3200	CRITICAL	ACE:A0	
353S00660	2	IC,CD3215,ACE,A1,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:A1	
353S00807	2	IC,CD3215,ACE,B0,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:B0	
353S00887	2	IC,CD3215,ACE,B0,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_B	(BOOT CODE: 0002.08.07)
353S00888	2	IC,CD3215,ACE,B0,USB PWR SW,OTP=2,BGA96	U3100,U3200	CRITICAL	ACE:B0_2	(BOOT CODE: 0002.08.07)
353S00926	2	IC,CD3215,ACE,B03,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_3	(BOOT CODE: 0002.08.08)
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:C0	

TBT ALPINE RIDGE

338S00160	1	IC,TBT,ALPINE RIDGE DP,QSJV,B1,6X6MM,BGA96	U2800	CRITICAL	TBT_AR:B1_QS
998-04160	1	IC,TBT,ALP-RIDGE DP,SLL44-TRAY,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ_TRAY
338S00176	1	IC,TBT,ALPN-RIDGE DP,SLL43-T&R,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ
338S00229	1	IC,TBT,ALPINE RIDGE,QSTY,QS,C0,CSP337	U2800	CRITICAL	TBT_AR:C0_QS
338S00249	1	IC,TBT,ALPINE RIDGE,QT5S,QS,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_QS
338S00254	1	IC,TBT,ALPINE RIDGE,SLLSM,PRQ,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_PRQ

WIRELESS MODULE

339S0250	1	MODULE,WIFI/BT,STELLA CIDRE,MUR,LGA80	U3700	CRITICAL	WIRELESS:MURATA
339S0251	1	MODULE,WIFI/BT,STELLA CIDRE,USI,LGA80	U3700	CRITICAL	WIRELESS:USI

Programmables (All Builds)

SMC

338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00334	1	IC,SMC-B1,EXT (V2.31A18) POC,X502	U5000	CRITICAL	SMC:POC
341S00429	1	IC,SMC-B1,EXT (V2.35A4) PROTO 1,X502	U5000	CRITICAL	SMC:PROTO1
341S00517	1	IC,SMC-B1,EXT (V2.35A51) PROTO 2,X502	U5000	CRITICAL	SMC:PROTO2
341S00562	1	IC,SMC-B1,EXT (V2.36A2) EVT,X502	U5000	CRITICAL	SMC:EVT
341S00611	1	IC,SMC-B1,EXT (V2.36A33) PRE-DVT,X502	U5000	CRITICAL	SMC:PREDVT
341S00633	1	IC,SMC-B1,EXT (V2.36A48) DVT,X502	U5000	CRITICAL	SMC:DVT
341S00662	1	IC,SMC-B1,EXT (V2.36F58) PVT,X502	U5000	CRITICAL	SMC:PVT

EFI ROM

335S0959	1	IC,SPI SERIAL FLASH,64M BITS,3V,CSP,QE=1	U6100	CRITICAL	BOOTROM:BLANK	MICRON
335S00006	335S0959	ALT_CMN	ALL	MACRONIX		
341S00389	1	IC,EFI (V0072) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO0	
341S00452	1	IC,EFI (V0093) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO1	
341S00513	1	IC,EFI (V0114) PROTO 2,X502	U6100	CRITICAL	BOOTROM:PROTO2	
341S00543	1	IC,EFI (V0130) PROTO 2.2,X502	U6100	CRITICAL	BOOTROM:PROTO2_2	
341S00573	1	IC,EFI (V0143) EVT,X502	U6100	CRITICAL	BOOTROM:EVT	
341S00673	1	IC,EFI (V0173) PVT,X502	U6100	CRITICAL	BOOTROM:PVT	

BT ROM

335S00024	1	IC,FLASH,USON8,512KBIT,75MHZ	U3770	CRITICAL	BT_ROM:BLANK
335S0837	335S00024	ALT_CMN	ALL	ALTERNATE	
341S00196	1	IC,BT ROM (V53) DVT,X261	U3770	CRITICAL	BT_ROM:X261
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PROTO0
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PVT

WIFI ROM

335S0956	1	IC,MEMORY,EEPROM,4K,1.7V-5.5V,UDFN8	U3780	CRITICAL	WIFI-ROM:BLANK
335S00145	335S0956	ALT_CMN	ALL	ALTERNATE	
341S00607	1	WIFI ROM (P175) PRE-DVT,WW1,X502	U3780	CRITICAL	WIFI-ROM:MURATA-FCC
341S00608	1	WIFI ROM (P175) PRE-DVT,WW2,X502	U3780	CRITICAL	WIFI-ROM:MURATA-ETSI
341S00609	1	WIFI ROM (P175) PRE-DVT,WW3,X502	U3780	CRITICAL	WIFI-ROM:MURATA-APAC
341S00610	1	WIFI ROM (P175) PRE-DVT,IND,X502	U3780	CRITICAL	WIFI-ROM:MURATA-IND
341S00636	1	WIFI ROM (P177) USI-WW1,X502	U3780	CRITICAL	WIFI-ROM:USI-FCC
341S00637	1	WIFI ROM (P177) USI-WW2,X502	U3780	CRITICAL	WIFI-ROM:USI-ETSI
341S00638	1	WIFI ROM (P177) USI-WW3,X502	U3780	CRITICAL	WIFI-ROM:USI-APAC
341S00639	1	WIFI ROM (P177) USI-IND,X502	U3780	CRITICAL	WIFI-ROM:USI-IND

TBT ROM

335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	AR_ROM:BLANK
341S00451	1	IC,NVM / AR (V0.8.15.E1) PROTO 1,X502	U2890	CRITICAL	AR_ROM:PROTO1
341S00512	1	IC,NVM (VB1-10.11-E2.6.3) PROTO 2,X502	U2890	CRITICAL	AR_ROM:PROTO2
341S00559	1	IC,NVM (V16.8) EVT,X502	U2890	CRITICAL	AR_ROM:EVT
341S00606	1	IC,NVM (V1.5) PRE-DVT,X502	U2890	CRITICAL	AR_ROM:PREDVT
341S00628	1	IC, NVM (V3.8), DVT, X502	U2890	CRITICAL	AR_ROM:DVT
341S00661	1	IC, NVM (VTBD), PVT, X502	U2890	CRITICAL	AR_ROM:PVT

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DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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BOM Configuration

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Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00101	4	IC,LPDDR3-1866,16GB,512MX32,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_8GB_1866
333S0784	4	IC,LPDDR3-1866,32GBIT,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_16GB_1866
333S00097	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_8GB_1866
333S00098	4	IC,LPDDR3-1866,32GB,1GX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_16GB_1866
333S00099	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_8GB_1866
333S00049	4	IC,SDRAM,LPDDR3-1866,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_16GB_1866

Main DRAM SPD Straps

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

	RAMCFG1	RAMCFG0
HYNIX	0 (STUFF R)	0 (STUFF R)
MICRON	0 (STUFF R)	1 (OPEN)
SAMSUNG	1 (OPEN)	0 (STUFF R)
-RESERVED-	1 (OPEN)	1 (OPEN)

	RAMCFG2
8GB	0 (STUFF R)
16GB	1 (OPEN)

	RAMCFG3
2133	0 (STUFF R)
1867	1 (OPEN)

	RAMCFG4
DIE A	0 (STUFF R)
DIE B	1 (OPEN)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0006	4	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1332,R1334		DRAM:HYNIX_8GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1334		DRAM:HYNIX_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1332,R1334		DRAM:MICRON_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1334		DRAM:MICRON_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1332,R1334		DRAM:SAMSUNG_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1334		DRAM:SAMSUNG_16GB_1866

MLB VERSION ID STRAPS

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE	INVERT TO VALUE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:POC	<11111>	<00000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:PROTO0	<11110>	<00001>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:PRE_PROTO1	<11101>	<00010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:PROTO1	<11100>	<00011>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:PROTO2	<11011>	<00100>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:PROTO2_2	<11010>	<00101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:EVT	<11001>	<00110>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:PREDVT	<11000>	<00111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:DVT	<10111>	<01000>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:DVT3	<10110>	<01001>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:PVT	<10101>	<01010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:PRQ1	<10100>	<01011>

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
107S00015	107S00011	ALT_CMN	ALL		TFT
107S00087	107S00029	ALT_CMN	ALL		YAGEO
107S00033	107S00034	ALT_CMN	ALL		TFT
107S00071	107S00053	ALT_CMN	ALL		YAGEO
107S00044	107S00076	ALT_CMN	ALL		CYNTEC
107S00070	107S0085	ALT_CMN	ALL		TDK
107S0248	107S0250	ALT_CMN	ALL		TFT
107S0249	107S0251	ALT_CMN	ALL		TFT
128S00009	128S00015	ALT_CMN	ALL		KEMET
128S00070	128S00015	ALT_CMN	ALL		PANASONIC
128S00010	128S00011	ALT_CMN	ALL		PANASONIC
128S00026	128S00011	ALT_CMN	ALL		NEC
128S00031	128S00011	ALT_CMN	ALL		ROHM
128S00058	128S00018	ALT_CMN	ALL		ROHM
128S00069	128S00067	ALT_CMN	ALL		ROHM
128S00062	128S00067	ALT_CMN	ALL		NEC
128S0364	128S0264	ALT_CMN	ALL		SANYO 2ND FACTORY
128S0311	128S0329	ALT_CMN	ALL		NEC ALT TO SANYO
128S0325	128S0397	ALT_CMN	ALL		PANASONIC
131S00134	131S00041	ALT_CMN	ALL		TAIYO YUDEN
132S00064	132S0409	ALT_CMN	ALL		MURATA
138S00077	138S00035	ALT_CMN	ALL		TAIYO YUDEN
138S00093	138S00035	ALT_CMN	ALL		KYOCERA
138S00084	138S00060	ALT_CMN	ALL		TAIYO YUDEN
138S0703	138S0648	ALT_CMN	ALL		MURATA
138S0700	138S0641	ALT_CMN	ALL		MURATA
138S0689	138S0701	ALT_CMN	ALL		MURATA
138S0864	138S0709	ALT_CMN	ALL		MULTIPLE
138S1103	138S0719	ALT_CMN	ALL		TAIYO YUDEN
138S0706	138S0739	ALT_CMN	ALL		MURATA
138S00106	138S0754	ALT_CMN	ALL		KYOCERA
138S00015	138S0777	ALT_CMN	ALL		MULTIPLE
138S0846	138S0811	ALT_CMN	ALL		SAMSUNG
138S00032	138S0831	ALT_CMN	ALL		TAIYO YUDEN
138S00049	138S0831	ALT_CMN	ALL		KYOCERA
138S0775	138S0860	ALT_CMN	ALL		SAMSUNG
138S00086	138S0884	ALT_CMN	ALL		TAIYO YUDEN
138S0738	138S1101	ALT_CMN	ALL		SAMSUNG
152S00381	152S1129	ALT_CMN	ALL		CHILISIN
152S00343	152S1682	ALT_CMN	ALL		MURATA
152S00363	152S00048	ALT_CMN	ALL		NEC
152S00358	152S00208	ALT_CMN	ALL		CHILISIN
152S00367	152S00266	ALT_CMN	ALL		NEC
152S00403	152S00322	ALT_CMN	ALL		CHILISIN
152S1872	152S00361	ALT_CMN	ALL		MURATA
155S0659	155S0382	ALT_CMN	ALL		MURATA
155S0694	155S0387	ALT_CMN	ALL		MURATA
155S00155	155S0441	ALT_CMN	ALL		TDK
155S0660	155S0513	ALT_CMN	ALL		MURATA
155S00007	155S0667	ALT_CMN	ALL		TAIYO YUDEN
155S00034	155S0706	ALT_CMN	ALL		MURATA
155S00203	155S0894	ALT_CMN	ALL		TAIYO YUDEN
155S00115	155S00114	ALT_CMN	ALL		MURATA

More Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
197S00046	197S00036	ALT_CMN	ALL		EPSON
197S00047	197S00036	ALT_CMN	ALL		KYOCERA
197S00048	197S00036	ALT_CMN	ALL		MURATA
197S00053	197S00050	ALT_CMN	ALL		KYOCERA
197S00054	197S00050	ALT_CMN	ALL		NDK
197S00055	197S00050	ALT_CMN	ALL		MURATA
311S00008	311S0271	ALT_CMN	ALL		DIODES INC
311S00060	311S0273	ALT_CMN	ALL		DIODES INC
311S00004	311S0370	ALT_CMN	ALL		ON SEMI
311S00013	311S0508	ALT_CMN	ALL		DIODES INC
311S00122	311S0543	ALT_CMN	ALL		DIODES INC
311S0596	311S0593	ALT_CMN	ALL		TI
311S00097	311S00036	ALT_CMN	ALL		DIODES INC
353S00711	353S2073	ALT_CMN	ALL		ON SEMI
353S00712	353S2216	ALT_CMN	ALL		ON SEMI
353S00107	353S3239	ALT_CMN	ALL		ON SEMI
353S00854	353S4342	ALT_CMN	ALL		ST MICRO
353S00769	353S4398	ALT_CMN	ALL		DIODES INC
353S00525	353S4471	ALT_CMN	ALL		VISHAY
371S0713	371S0558	ALT_CMN	ALL		DIODES INC
371S00074	371S0602	ALT_CMN	ALL		INFINEON
371S0704	371S00077	ALT_CMN	ALL		NXP
371S00089	371S00085	ALT_CMN	ALL		DIODES INC
372S0186	372S0185	ALT_CMN	ALL		NXP
372S00016	372S00015	ALT_CMN	ALL		DIODES INC
376S1053	376S0604	ALT_CMN	ALL		DIODES INC
376S1106	376S0678	ALT_CMN	ALL		FAIRCHILD
376S00014	376S0761	ALT_CMN	ALL		TOSHIBA
376S00086	376S0761	ALT_CMN	ALL		DIODES INC.
376S1080	376S0820	ALT_CMN	ALL		DIODES INC
376S00074	376S0855	ALT_CMN	ALL		TOSHIBA
376S00146	376S1061	ALT_CMN	ALL		ROHM
376S1089	376S1128	ALT_CMN	ALL		NXP
377S00031	377S0178	ALT_CMN	ALL		ON SEMI
377S00048	377S00017	ALT_CMN	ALL		ST MICRO
377S0155	377S00011	ALT_CMN	ALL		ON SEMI
740S0144	740S0118	ALT_CMN	ALL		LITTELFUSE
740S00028	740S0118	ALT_CMN	ALL		BUSSMANN
740S00003	740S0135	ALT_CMN	ALL		AEM, INC.
740S00027	740S0159	ALT_CMN	ALL		BOURNS
740S00033	740S00002	ALT_CMN	ALL		THINKING
740S00007	740S00019	ALT_CMN	ALL		BOURNS

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qq群： 241000

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE
BOM Configuration

Apple Inc.

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MOUNTING HOLES

998-03850

SH0400
4.0R3.6-NSP

SH0401
4.0R3.6-NSP

FAN MOUNTING HOLE

998-03850

SH0410
TH-NSP
SL-2.6X2.0-4.7X4.1

PLATED HOLES

SH0420
TH-NSP
LARGER SLOT, NEAR ANTENNA
SL-3.38X2.1-5.88X4.6
998-06494

SH0421
TH-NSP
SL-3.36X2.1-5.86X4.6
998-03823

SH0425
TH-NSP
SL-3.36X2.1-5.86X4.6

SH0426
TH-NSP
SL-3.36X2.1-5.86X4.6
998-03823

POGO PINS

870-01680

SH0430
POGO-2.30D-4.1H-SM

SH0431
POGO-2.30D-4.1H-SM

SH0434
POGO-2.30D-4.1H-SM

SH0435
POGO-2.30D-4.1H-SM

870-02068

SH0437
POGO-2.30D-4.1H-SM

SH0432
POGO-2.00D-2.95H-SM-1

SH0436
POGO-2.30D-4.1H-SM

SH0433
POGO-2.00D-2.95H-SM-1

TOP STANDOFFS

860-00385

SH0450
2.8OD1.2ID-1.44H-SM

SH0451
2.8OD1.2ID-1.44H-SM

SH0452
2.8OD1.2ID-1.44H-SM

SH0453
2.8OD1.2ID-1.44H-SM

SH0455
2.8OD1.2ID-1.44H-SM

SH0457
2.8OD1.2ID-1.44H-SM

BOTTOM STANDOFFS

860-00468

SH0460
2.8OD1.2ID-3.0H-SM

SH0461
2.8OD1.2ID-3.0H-SM

SHIELD CANS

MEMORY CAN - TOP

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07887	1	SHIELD CAN FENCE,DRAM,MN,X520	SHLD4	CRITICAL	SHIELD_CAN_MEMORY_TOP

MEMORY CAN - BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08894	1	SHIELD FENCE,BOT DRAM,SUS,PRE-MN,X520	SHLD1	CRITICAL	SHIELD_CAN_MEMORY_BOT

WIRELESS CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07886	1	SHIELD CAN FENCE,WIFI,SYM,MN,TALL,X520	SHLD2	CRITICAL	SHIELD_CAN_WIFI

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qq群： 241000

USB-C CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07885	1	SHIELD CAN,AR,USB-C,THRU,X520	SHLD3	CRITICAL	SHIELD_CAN_USBC

BOM_COST_GROUP=MECHANICALS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PD Parts

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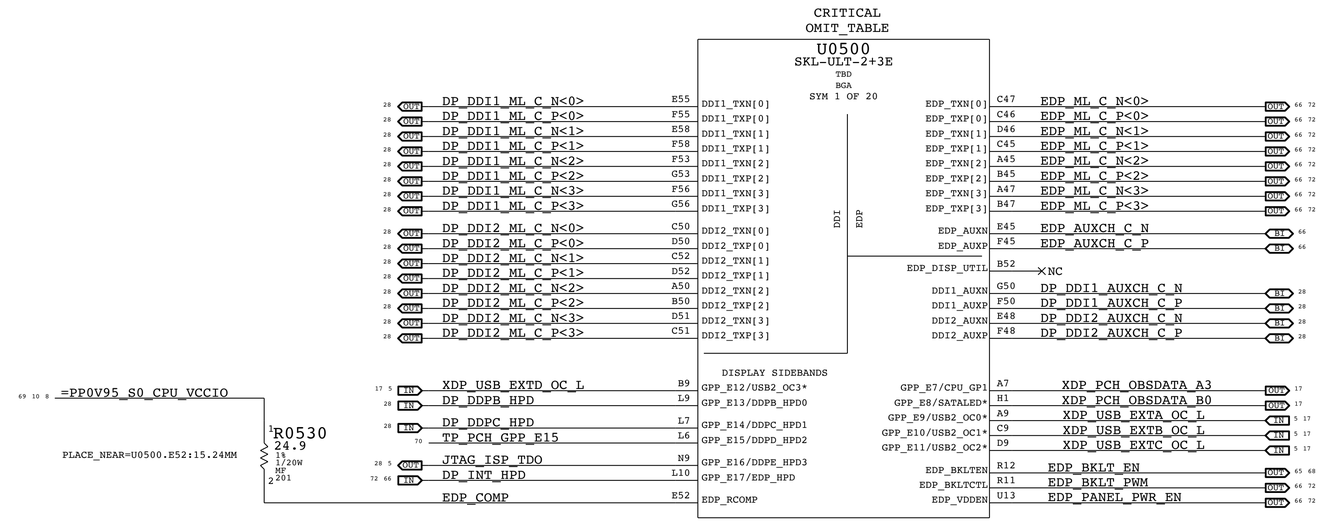

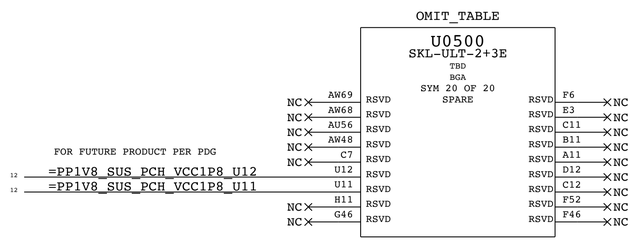

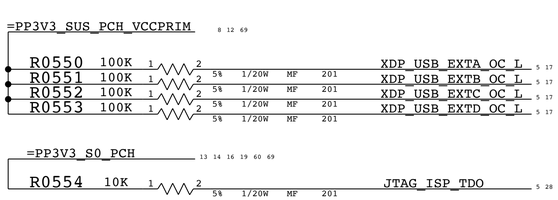

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BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
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CPU GFX

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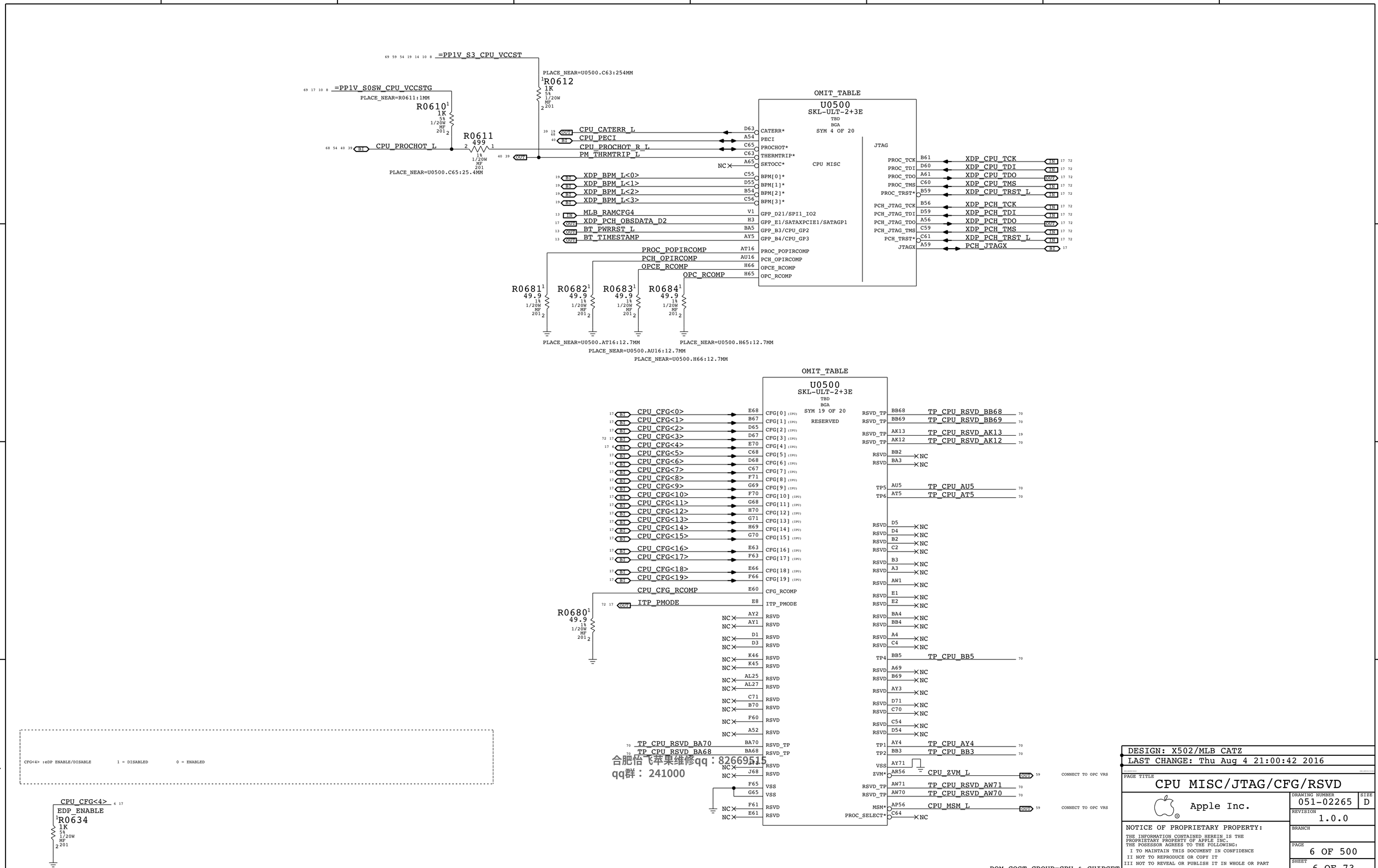

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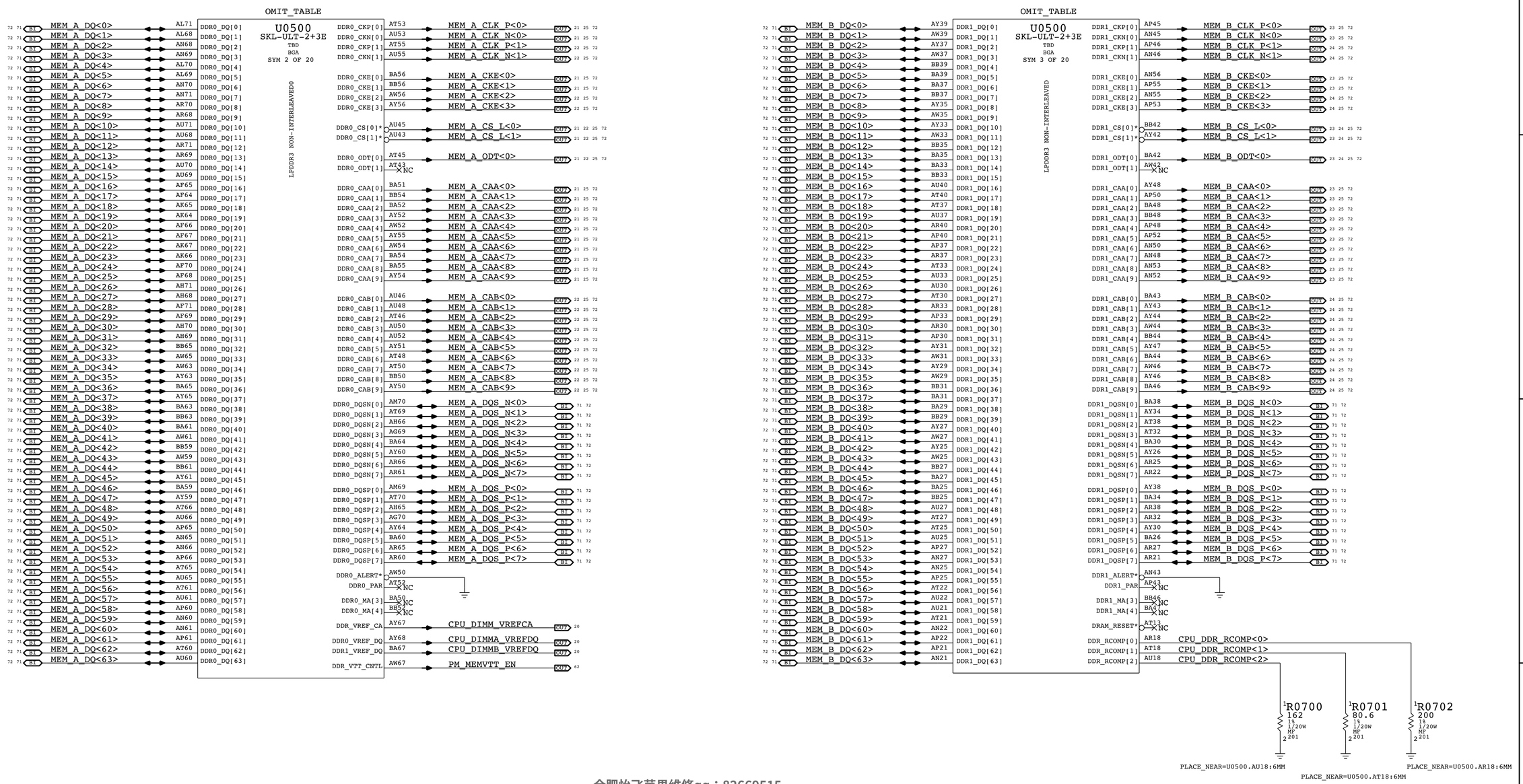

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qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

CPU LPDDR3 Interface

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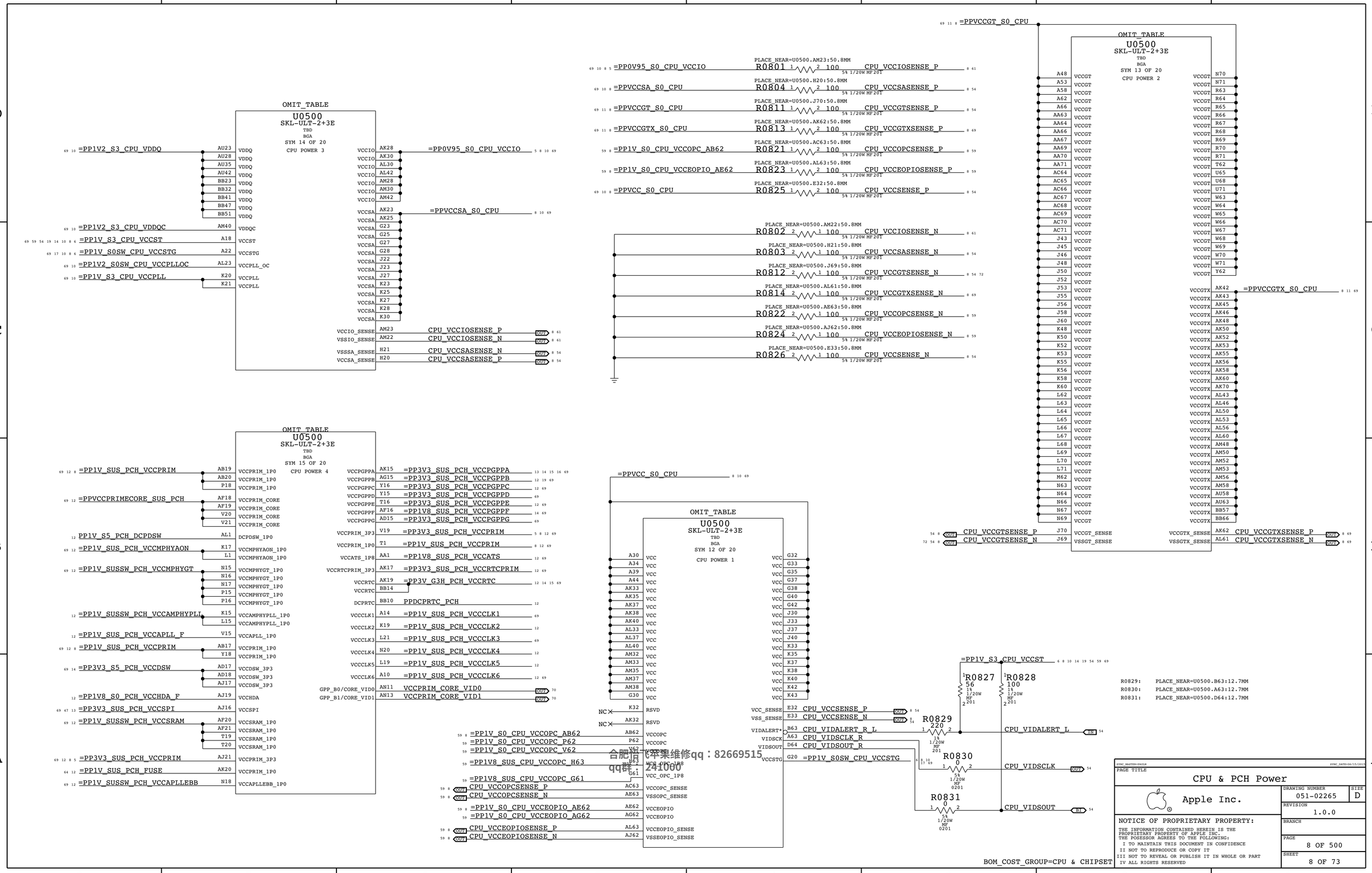
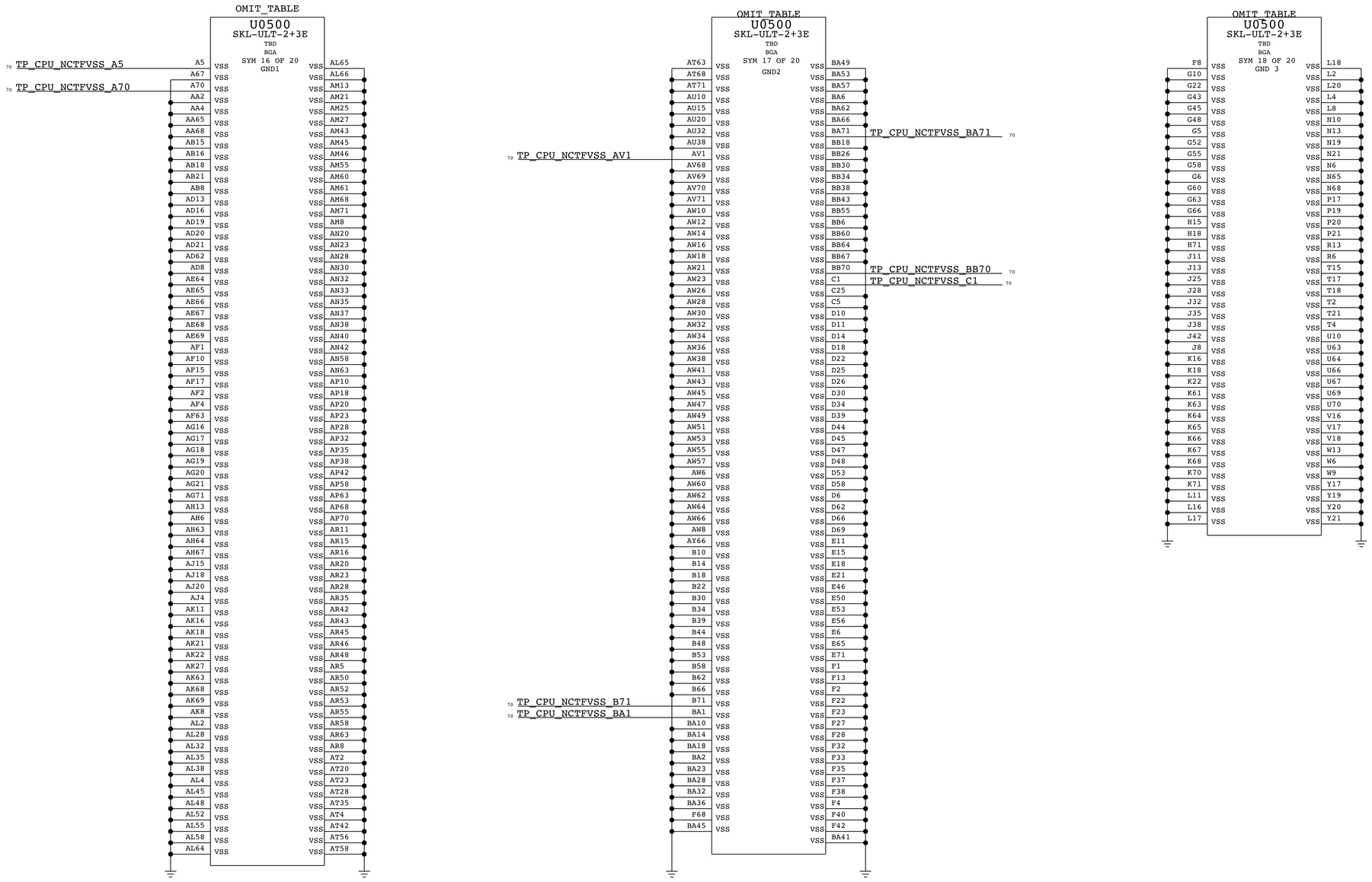


合肥维修苹果维修qq：82669515
qq群：241000



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qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

CPU & PCH Grounds

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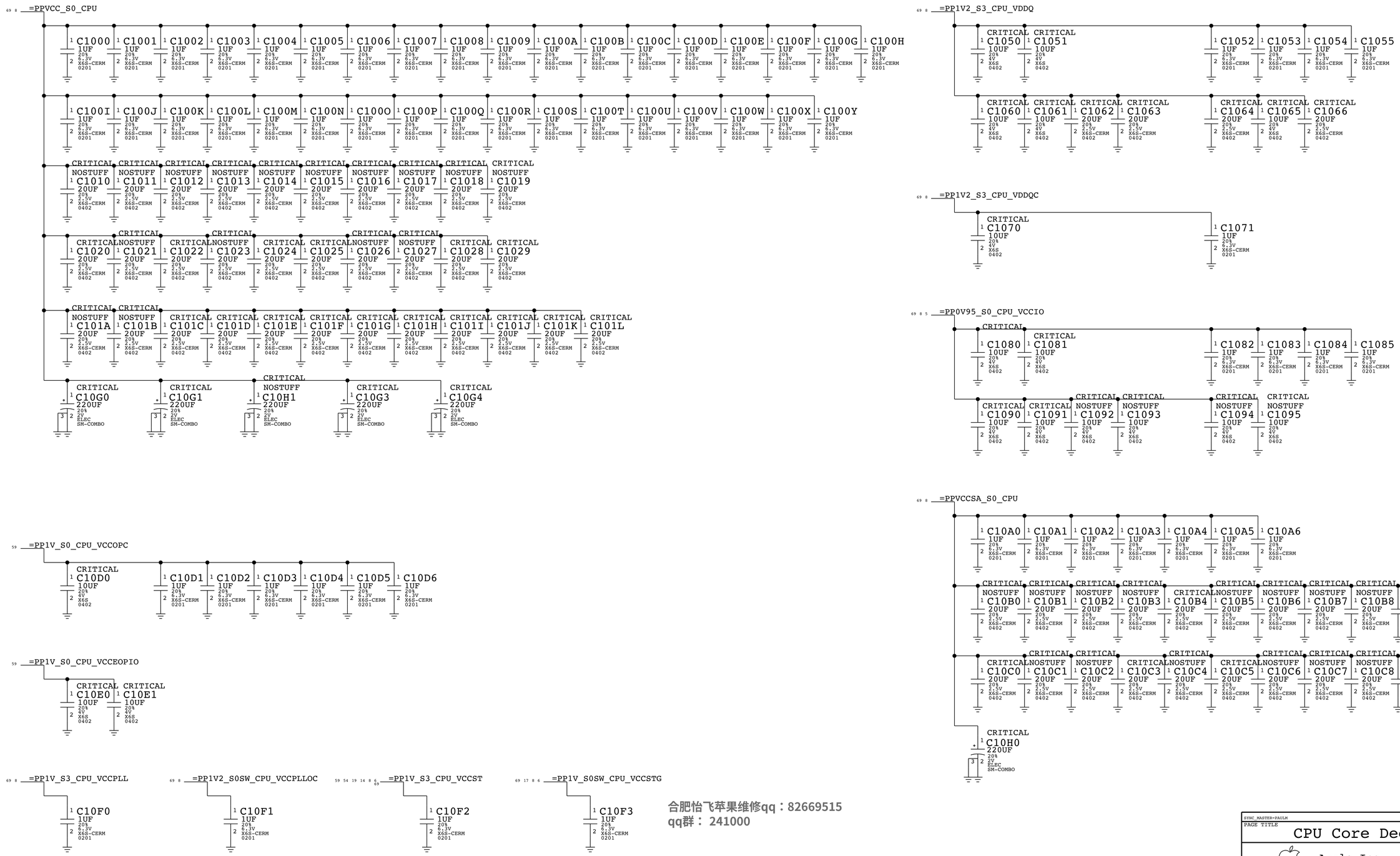

合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE
CPU Core Decoupling

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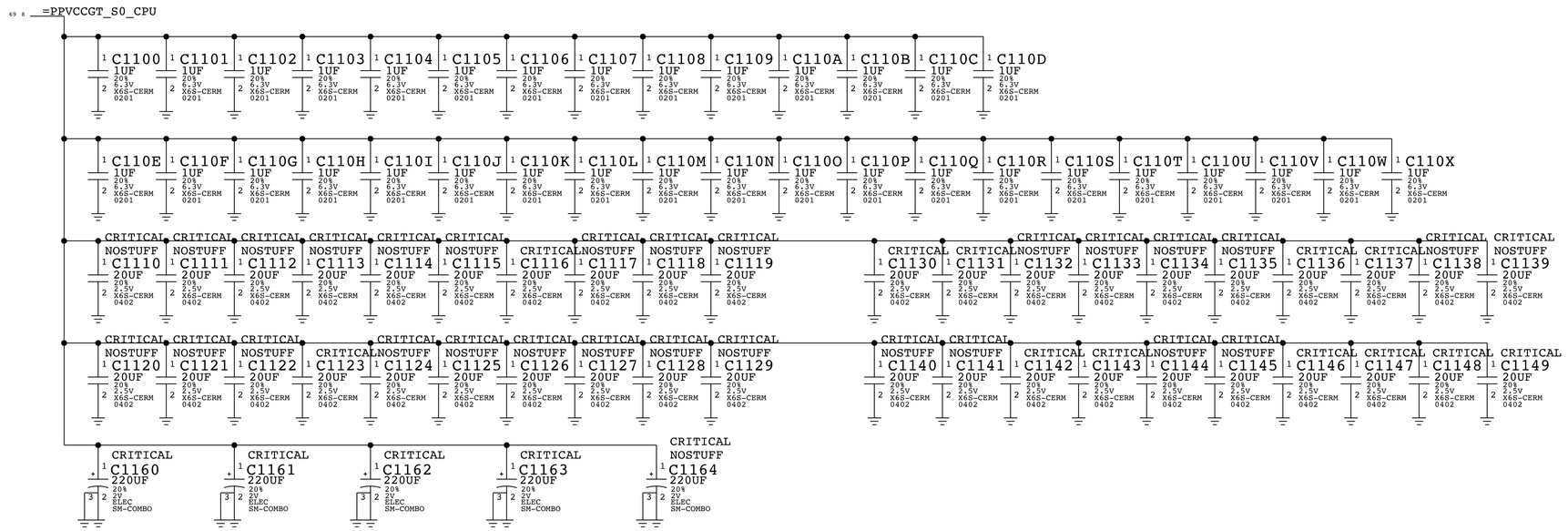

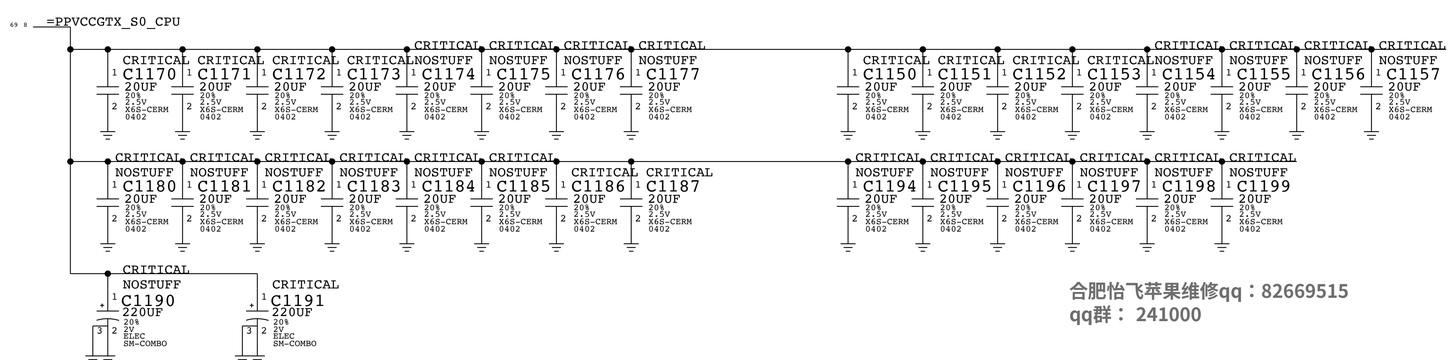

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qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU GT Decoupling

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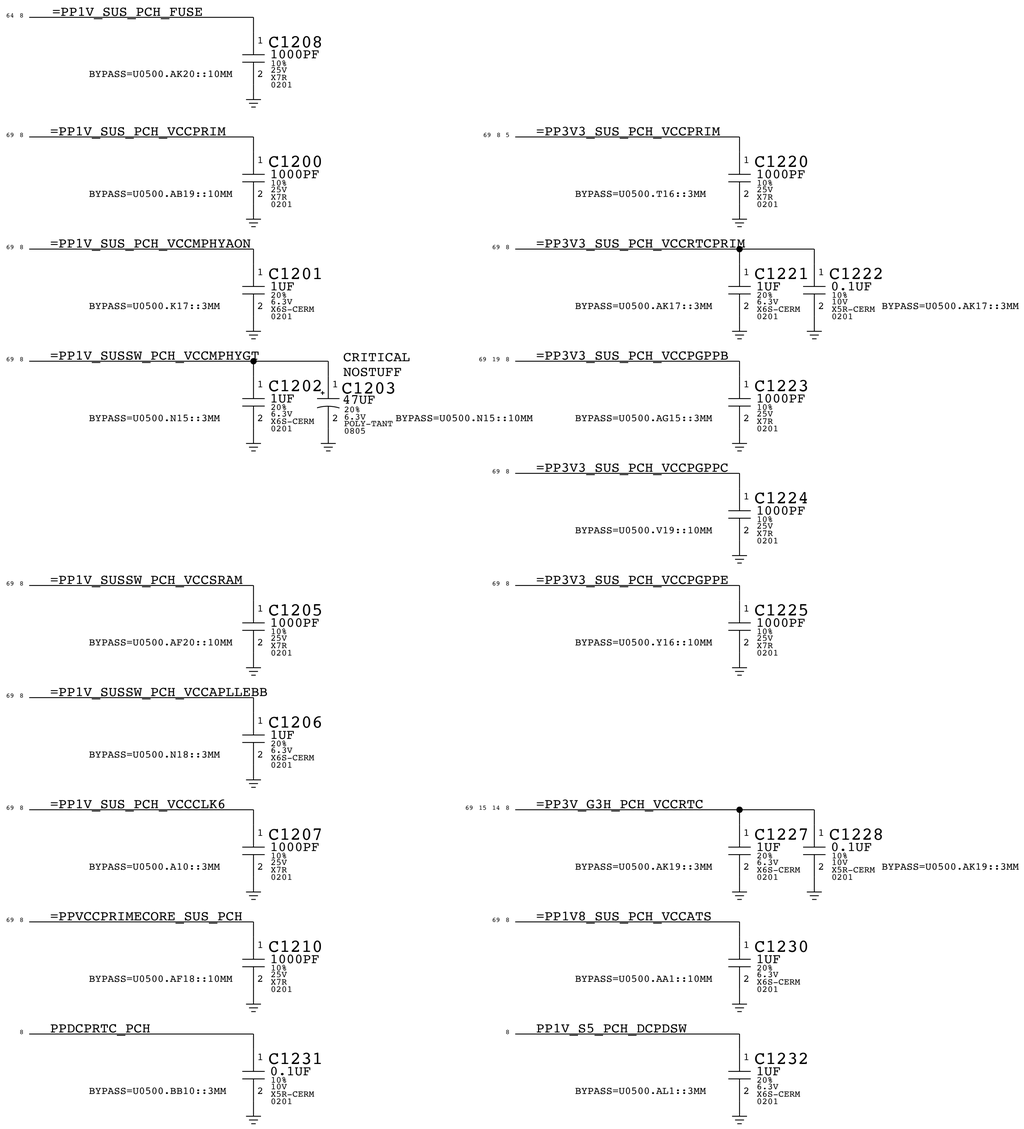
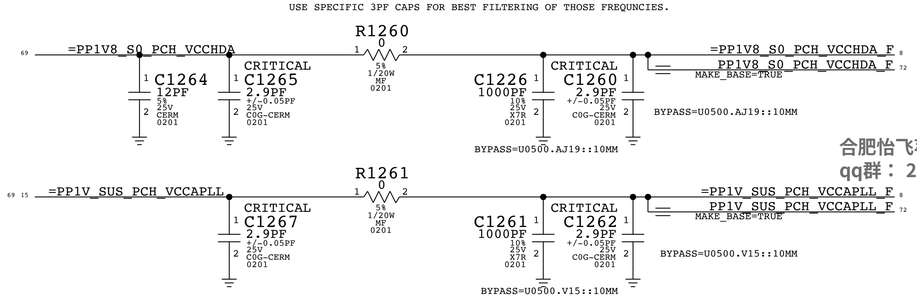
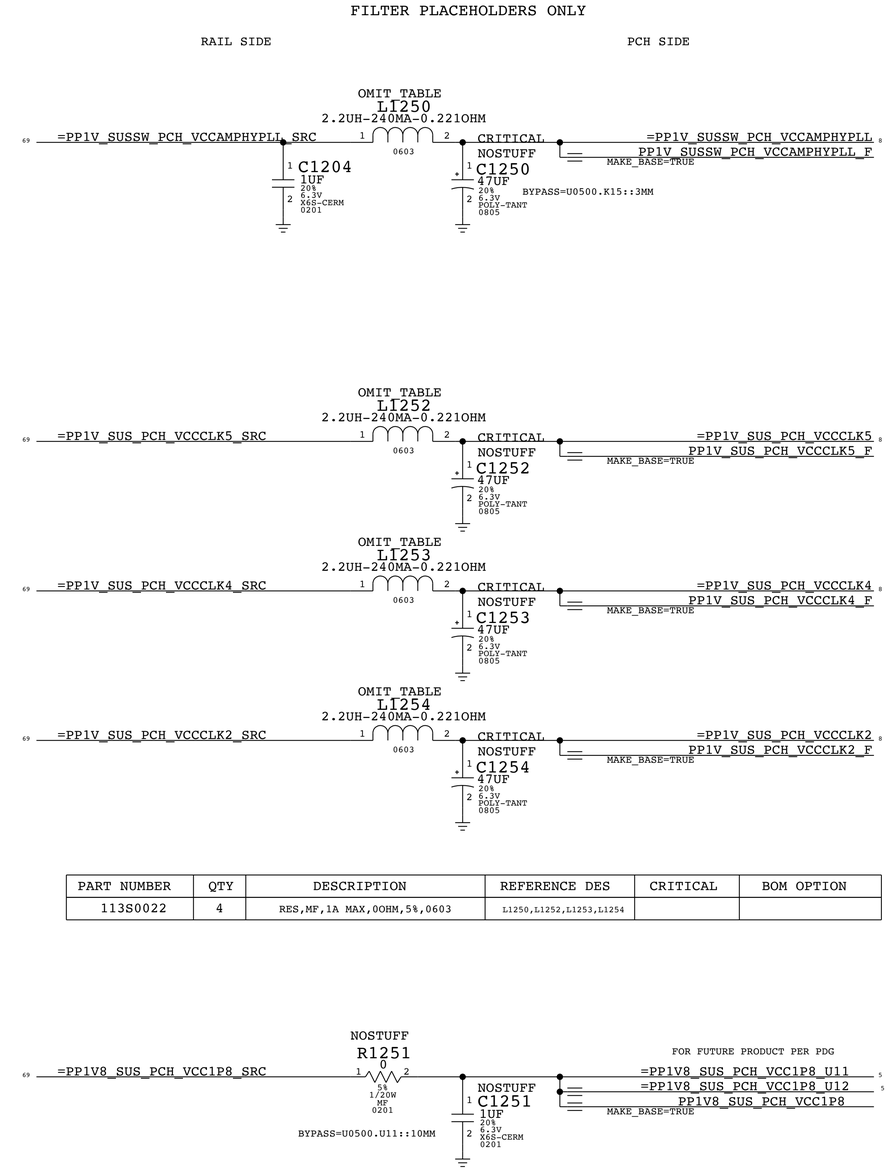


CPU CIRCUITS GENERATE NOISE AT WIFI BAND FREQUENCIES.
USE SPECIFIC 3PF CAPS FOR BEST FILTERING OF THOSE FREQUNCIES.



FILTER PLACEHOLDERS ONLY



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,0OHM,5%,0603	L1250,L1252,L1253,L1254		

BOM_COST_GROUP=CPU & CHIPSET

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qq群： 241000

PAGE TITLE
PCH Decoupling

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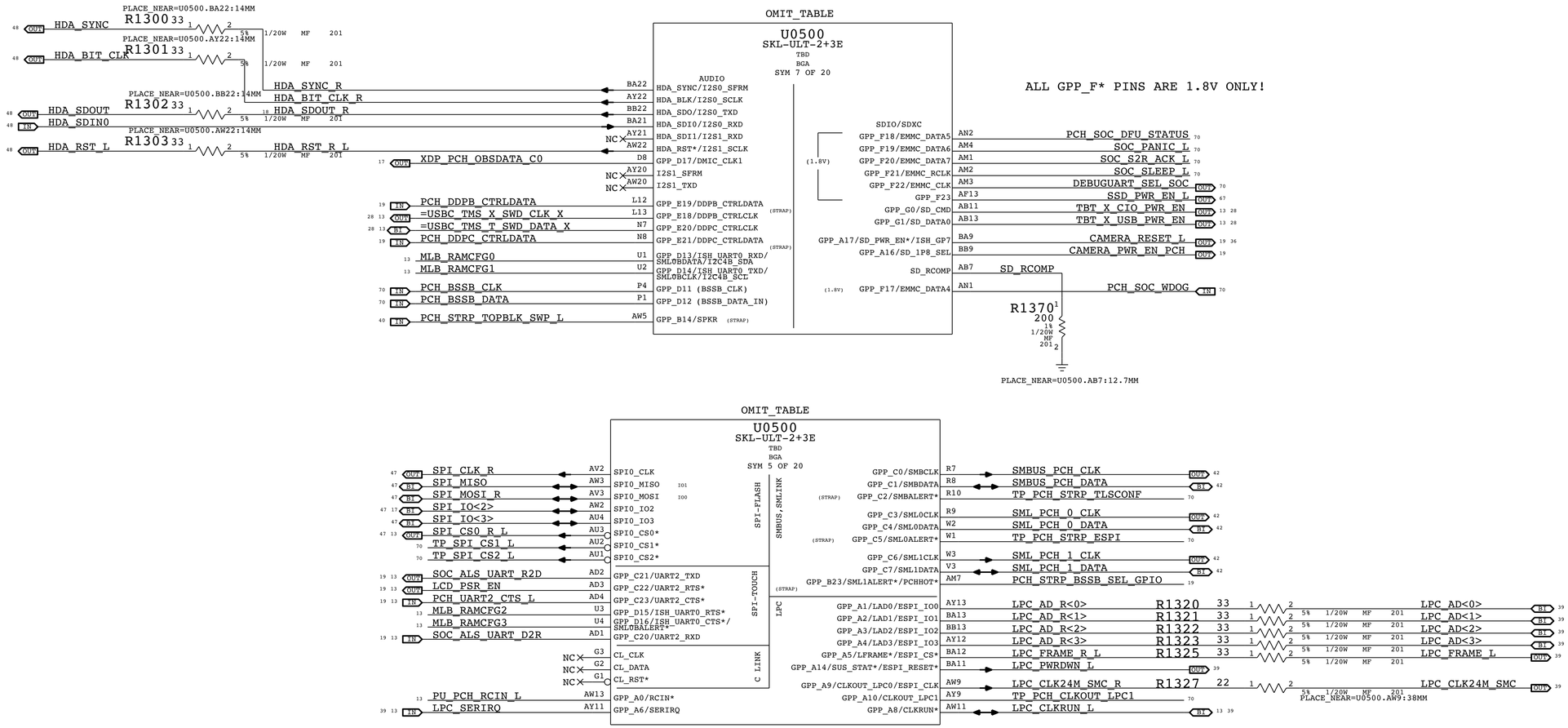
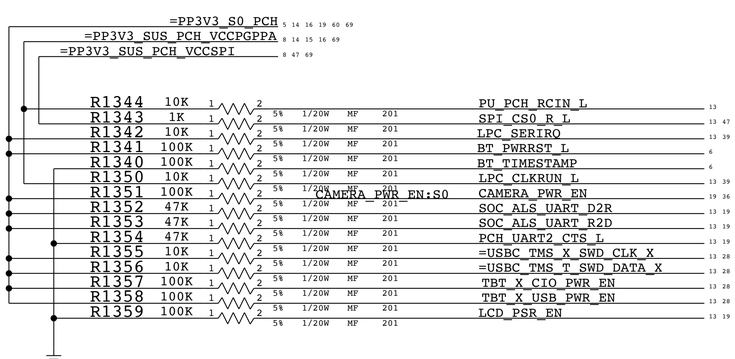
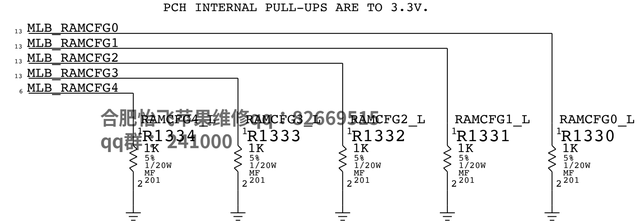




MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



合肥兴子苹果维修 13266915
qq号 241000

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH Audio/LPC/SPI/SMBus

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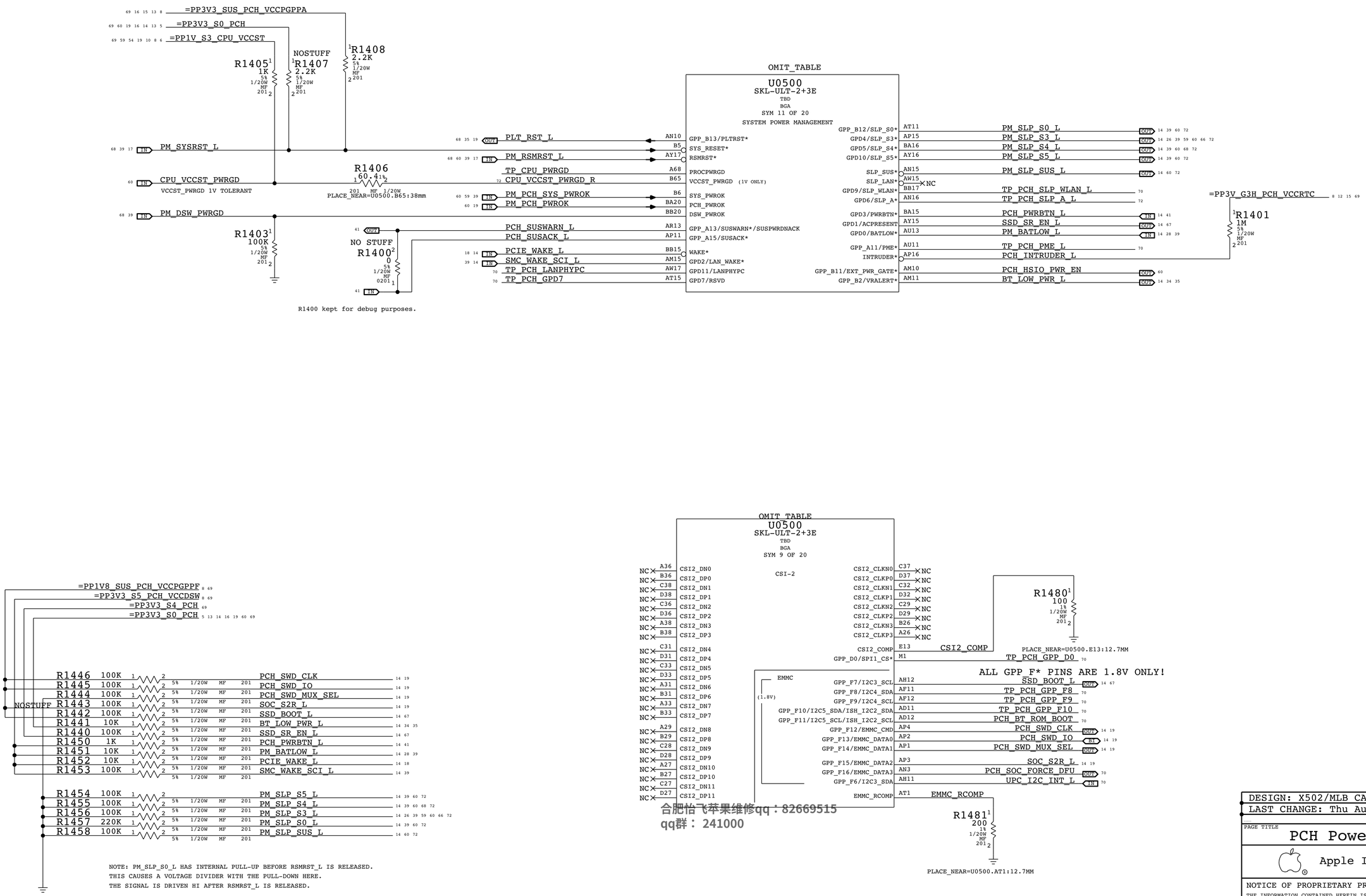
PCH Reset Button



合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH Power Management

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PCIe Port Assignments:

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

Port	Net	Pin	Signal	Dir
SSD LANE 0	PCIE_SSD_D2R_N<0>	H13	PCIE1_RXN/USB3_5_RXN	IN
	PCIE_SSD_D2R_P<0>	G13	PCIE1_RXP/USB3_5_RXP	IN
	PCIE_SSD_R2D_C_N<0>	B17	PCIE1_TXN/USB3_5_TXN	OUT
	PCIE_SSD_R2D_C_P<0>	A17	PCIE1_TXP/USB3_5_TXP	OUT
SSD LANE 1	PCIE_SSD_D2R_N<1>	G11	PCIE2_RXN/USB3_6_RXN	IN
	PCIE_SSD_D2R_P<1>	F11	PCIE2_RXP/USB3_6_RXP	IN
	PCIE_SSD_R2D_C_N<1>	D16	PCIE2_TXN/USB3_6_TXN	OUT
	PCIE_SSD_R2D_C_P<1>	C16	PCIE2_TXP/USB3_6_TXP	OUT
SSD LANE 2	PCIE_SSD_D2R_N<2>	H16	PCIE3_RXN	IN
	PCIE_SSD_D2R_P<2>	G16	PCIE3_RXP	IN
	PCIE_SSD_R2D_C_N<2>	D17	PCIE3_TXN	OUT
	PCIE_SSD_R2D_C_P<2>	C17	PCIE3_TXP	OUT
SSD LANE 3	PCIE_SSD_D2R_N<3>	G15	PCIE4_RXN	IN
	PCIE_SSD_D2R_P<3>	F15	PCIE4_RXP	IN
	PCIE_SSD_R2D_C_N<3>	B19	PCIE4_TXN	OUT
	PCIE_SSD_R2D_C_P<3>	A19	PCIE4_TXP	OUT
Thunderbolt X lane 0	PCIE_TBT_X_D2R_N<0>	F16	PCIE5_RXN	IN
	PCIE_TBT_X_D2R_P<0>	E16	PCIE5_RXP	IN
	PCIE_TBT_X_R2D_C_N<0>	C19	PCIE5_TXN	OUT
	PCIE_TBT_X_R2D_C_P<0>	D19	PCIE5_TXP	OUT
Thunderbolt X lane 1	PCIE_TBT_X_D2R_N<1>	G18	PCIE6_RXN	IN
	PCIE_TBT_X_D2R_P<1>	F18	PCIE6_RXP	IN
	PCIE_TBT_X_R2D_C_N<1>	D20	PCIE6_TXN	OUT
	PCIE_TBT_X_R2D_C_P<1>	C20	PCIE6_TXP	OUT
Thunderbolt X lane 2	PCIE_TBT_X_D2R_N<2>	F20	PCIE7_RXN/SATA0_RXN	IN
	PCIE_TBT_X_D2R_P<2>	E20	PCIE7_RXP/SATA0_RXP	IN
	PCIE_TBT_X_R2D_C_N<2>	B21	PCIE7_TXN/SATA0_TXN	OUT
	PCIE_TBT_X_R2D_C_P<2>	A21	PCIE7_TXP/SATA0_TXP	OUT
Thunderbolt X lane 3	PCIE_TBT_X_D2R_N<3>	G21	PCIE8_RXN/SATA1A_RXN	IN
	PCIE_TBT_X_D2R_P<3>	F21	PCIE8_RXP/SATA1A_RXP	IN
	PCIE_TBT_X_R2D_C_N<3>	D21	PCIE8_TXN/SATA1A_TXN	OUT
	PCIE_TBT_X_R2D_C_P<3>	C21	PCIE8_TXP/SATA1A_TXP	OUT
AirPort	PCIE_AP_D2R_N	E22	PCIE9_RXN	IN
	PCIE_AP_D2R_P	E23	PCIE9_RXP	IN
	PCIE_AP_R2D_C_N	B23	PCIE9_TXN	OUT
	PCIE_AP_R2D_C_P	A23	PCIE9_TXP	OUT
CAMERA	PCIE_CAMERA_D2R_N	F25	PCIE10_RXN	IN
	PCIE_CAMERA_D2R_P	E25	PCIE10_RXP	IN
	PCIE_CAMERA_R2D_C_N	D23	PCIE10_TXN	OUT
	PCIE_CAMERA_R2D_C_P	C23	PCIE10_TXP	OUT
	PCH_PCIE_RCOMP_N	F5	PCIE_RCOMPN	
	PCH_PCIE_RCOMP_P	E5	PCIE_RCOMPP	
	XDP_CPU_PRDY_L	D56	PROC_PRDY*	OUT
	XDP_CPU_PREQ_L	D61	PROC_PREQ*	IN
	SMC_RUNTIME_SCI_L	BB11	GPP_A7/PIRQA*	IN
Thunderbolt T lane 0	PCIE_TBT_T_D2R_N<0>	E28	PCIE11_RXN/SATA1B_RXN	IN
	PCIE_TBT_T_D2R_P<0>	E27	PCIE11_RXP/SATA1B_RXP	IN
	PCIE_TBT_T_R2D_C_N<0>	D24	PCIE11_TXN/SATA1B_TXN	OUT
	PCIE_TBT_T_R2D_C_P<0>	C24	PCIE11_TXP/SATA1B_TXP	OUT
Thunderbolt T lane 1	PCIE_TBT_T_D2R_N<1>	E30	PCIE12_RXN/SATA2_RXN	IN
	PCIE_TBT_T_D2R_P<1>	F30	PCIE12_RXP/SATA2_RXP	IN
	PCIE_TBT_T_R2D_C_N<1>	A25	PCIE12_TXN/SATA2_TXN	OUT
	PCIE_TBT_T_R2D_C_P<1>	B25	PCIE12_TXP/SATA2_TXP	OUT

PCIE/USB3/SATA

R1504 100 1% 1/20W MF 201

Net	Pin	Signal
USB3_1_RXN	H8	USB3_EXTA_D2R_N
USB3_1_RXP	G8	USB3_EXTA_D2R_P
USB3_1_TXN	C13	USB3_EXTA_R2D_C_N
USB3_1_TXP	D13	USB3_EXTA_R2D_C_P
USB3_2_RXN/SSIC_RXN	J6	USB3_EXTB_D2R_N
USB3_2_RXP/SSIC_RXP	H6	USB3_EXTB_D2R_P
USB3_2_TXN/SSIC_TXN	B13	USB3_EXTB_R2D_C_N
USB3_2_TXP/SSIC_TXP	A13	USB3_EXTB_R2D_C_P
USB3_3_RXN	J10	TP_USB3_03_D2RN
USB3_3_RXP	H10	TP_USB3_03_D2RP
USB3_3_TXN	B15	TP_USB3_03_R2DN
USB3_3_TXP	A15	TP_USB3_03_R2DP
USB3_4_RXN	E10	TP_USB3_04_D2RN
USB3_4_RXP	F10	TP_USB3_04_D2RP
USB3_4_TXN	C15	TP_USB3_04_R2DN
USB3_4_TXP	D15	TP_USB3_04_R2DP
USB2N_1	AB9	USB_EXTA_N
USB2P_1	AB10	USB_EXTA_P
USB2N_2	AD6	USB_EXTB_N
USB2P_2	AD7	USB_EXTB_P
USB2N_3	AH3	USB_CAMERA_DFR_N
USB2P_3	AJ3	USB_CAMERA_DFR_P
USB2N_4	AD9	TP_USB_TESTERN
USB2P_4	AD10	TP_USB_TESTERP
USB2N_5	AJ1	NC_USB2_05N
USB2P_5	AJ2	NC_USB2_05P
USB2N_6	AF6	NC_USB2_06N
USB2P_6	AF7	NC_USB2_06P
USB2N_7	AH1	NC_USB2_07N
USB2P_7	AH2	NC_USB2_07P
USB2N_8	AF8	NC_USB2_08N
USB2P_8	AF9	NC_USB2_08P
USB2N_9	AG1	NC_USB2_09N
USB2P_9	AG2	NC_USB2_09P
USB2N_10	AH7	NC_USB2_10N
USB2P_10	AH8	NC_USB2_10P
USB2_COMP	AB6	PCH_USB2_COMP
USB2_ID	AG3	
USB2_VBUSSENSE	AG4	PCH_USB2_VBUSSENSE
GPP_E3/CPU_GP0	A6	XDP_PCH_OBSFN_C1
GPP_E4/DEVSLP0	J1	XDP_JTAG_ISP_TCK
GPP_E5/DEVSLP1	J2	XDP_JTAG_ISP_TDI
GPP_E6/DEVSLP2	J3	XDP_PCH_OBSDATA_A2
GPP_D22/SPI1_IO3	V2	SPKR_ID0
GPP_D23/I2S_MCLK	J5	XDP_PCH_OBSDATA_D0
GPP_E0/SATAXPCIE0/SATAGP0	H2	XDP_PCH_OBSDATA_D1
GPP_D18/DMIC_DATA1	C8	XDP_PCH_OBSDATA_C1
GPP_D19/DMIC_CLK0	H5	XDP_PCH_OBSDATA_C2
GPP_D20/DMIC_DATA0	D7	XDP_PCH_OBSDATA_C3
GPP_E2/SATAXPCIE2/SATAGP2	G4	XDP_PCH_OBSDATA_D3

SSIC/USB3

USB2

EXT A (SS,DCI)

EXT B (SS)

EXT A (LS/FS/HS)

EXT B (LS/FS/HS)

GROUNDED PER SKYLAKE MOW 2015WW10.

R1503 1K 5% 1/20W MF 201

PLACE_NEAR=U0500.AG4:12.7MM

R1501 113 1% 1/20W MF 201

PLACE_NEAR=U0500.AB6:12.7MM

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20

CLOCK SIGNALS

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

Net	Pin	Signal	Dir
PCIE_CLK100M_SSD_N	D42	CLKOUT_PCIE_N0	OUT
PCIE_CLK100M_SSD_P	C42	CLKOUT_PCIE_P0	OUT
=SSD_CLKREQ_L	AR10	GPP_B5/SRCCLKREQ0*	IN
PCIE_CLK100M_TBT_X_N	B42	CLKOUT_PCIE_N1	OUT
PCIE_CLK100M_TBT_X_P	A42	CLKOUT_PCIE_P1	OUT
=TBT_X_CLKREQ_L	AT7	GPP_B6/SRCCLKREQ1*	IN
PCIE_CLK100M_TBT_T_N	D41	CLKOUT_PCIE_N2	OUT
PCIE_CLK100M_TBT_T_P	C41	CLKOUT_PCIE_P2	OUT
=TBT_T_CLKREQ_L	AT8	GPP_B7/SRCCLKREQ2*	IN
PCIE_CLK100M_AP_N	D40	CLKOUT_PCIE_N3	OUT
PCIE_CLK100M_AP_P	C40	CLKOUT_PCIE_P3	OUT
=AP_CLKREQ_L	AT10	GPP_B8/SRCCLKREQ3*	IN
PCIE_CLK100M_CAMERA_N	B40	CLKOUT_PCIE_N4	OUT
PCIE_CLK100M_CAMERA_P	A40	CLKOUT_PCIE_P4	OUT
=CAMERA_CLKREQ_L	AU8	GPP_B9/SRCCLKREQ4*	IN
TP_PCIE_CLK100M5N	E40	CLKOUT_PCIE_N5	OUT
TP_PCIE_CLK100M5P	E38	CLKOUT_PCIE_P5	OUT
TP_PCH_CLKREQ5_L	AU7	GPP_B10/SRCCLKREQ5*	IN
CLKOUT_ITPXDP_N	F43	TP_ITPXDP_CLK100MN	
CLKOUT_ITPXDP_P	E43	TP_ITPXDP_CLK100MP	
GPD8/SUSCLK	BA17	PM_CLK32K_SUSCLK_R	OUT
XTAL24_IN	E37	PCH_CLK24M_XTALIN	IN
XTAL24_OUT	E35	PCH_CLK24M_XTALOUT	OUT
XCLK_BIASREF	E42	PCH_DIFFCLK_BIASREF	
RTCX1	AM18	PCH_CLK32K_RTCX1	IN
RTCX2	AM20	PCH_CLK32K_RTCX2	OUT
SRTCRST*	AN18	PCH_SRTCRST_L	
RTCRST*	AM16	RTC_RESET_L	

=PP1V_SUS_PCH_VCCAPLL

PLACE_NEAR=U0500.E42:2.54mm

R1520 2.7K 1% 1/20W MF 201

=PP3V_G3H_PCH_VCCRTC

R1530 20K 1% 1/20W MF 201

R1531 20K 1% 1/20W MF 201

C1530 1UF 20% 6.3V X6S-CERM 0201

C1531 1UF 20% 6.3V X6S-CERM 0201

=PP3V3_SUS_PCH_VCCPGPPA

R1550 100K 5% 1/20W MF 201

SMC_RUNTIME_SCI_L

品质为王苹果维修qq：82669515
电话：13761241000

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH PCIE/USB/CLKS

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ALL GPP_F* PINS ARE 1.8V ONLY!
OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 6 OF 20

			LPSS			ISH		
19 16 OUT	AUD_SPI_CS_L	AN8	GPP_B15/GSPI0_CS*		M4	GPP_D5/ISH_I2C0_SDA	MLB_BOARD_ID0	16
19 16 OUT	AUD_SPI_CLK	AP7	GPP_B16/GSPI0_CLK		N3	GPP_D6/ISH_I2C0_SCL	MLB_BOARD_ID1	16
19 16 IN	AUD_SPI_MISO	AP8	GPP_B17/GSPI0_MISO		N1	GPP_D7/ISH_I2C1_SDA	MLB_BOARD_ID2	16
19 16 OUT	AUD_SPI_MOSI	AR7	GPP_B18/GSPI0_MOSI	(STRAP)	N2	GPP_D8/ISH_I2C1_SCL	MLB_BOARD_ID3	16
38 16 OUT	TPAD_SPI_CS_L	AM5	GPP_B19/GSPI1_CS*		M2	GPP_D1/SPI1_CLK	TP_PCH_GPP_D1	70
72 38 16 OUT	TPAD_SPI_CLK	AN7	GPP_B20/GSPI1_CLK		M3	GPP_D2/SPI1_MISO	SPKR_ID1	19
72 38 16 IN	TPAD_SPI_MISO	AP5	GPP_B21/GSPI1_MISO		J4	GPP_D3/SPI1_MOSI	TP_PCH_GPP_D3	70
72 38 16 OUT	TPAD_SPI_MOSI	AN5	GPP_B22/GSPI1_MOSI	(STRAP)	B7	GPP_D4/FLASHTRIG	TP_PCH_GPP_D4	70
35 16 IN	PCH_BT_UART_D2R	AB1	GPP_C8/UART0_RXD		AH9	GPP_F4/I2C2_SDA (1.8V)	I2C_UPC_SDA BI	70
35 16 OUT	PCH_BT_UART_R2D	AB2	GPP_C9/UART0_TXD		AH10	GPP_F5/I2C2_SCL (1.8V)	I2C_UPC_SCL OUT	70
35 16 OUT	PCH_BT_UART_RTS_L	W4	GPP_C10/UART0_RTS*		W8	GPP_G6/SD_CLK	AP_RESET_L OUT	19 34 35
35 16 IN	PCH_BT_UART_CTS_L	AB3	GPP_C11/UART0_CTS*		P2	GPP_D9	MLB_BOARD_ID4	16
18 16 OUT	AP_S0IX_WAKE_SEL	U7	GPP_C16/I2C0_SDA		P3	GPP_D10	MLB_DEV_L IN	70
18 16 IN	AP_S0IX_WAKE_L	U6	GPP_C17/I2C0_SCL		W7	GPP_G7/SD_WP	AP_DEV_WAKE OUT	16 34 35
28 16 IN	TBT_X_PLUG_EVENT_L	U8	GPP_C18/I2C1_SDA		AB12	GPP_G2/SD_DATA1	TBT_T_CIO_PWR_EN OUT	70
19 16 IN	TBT_T_PLUG_EVENT_L	U9	GPP_C19/I2C1_SCL		W12	GPP_G3/SD_DATA2	TBT_T_USB_PWR_EN OUT	70
19 16 IN	SOC_UART_D2R	AC1	GPP_C12/UART1_RXD/ISH_UART1_RXD		W11	GPP_G4/SD_DATA3	TBT_X_PCI_RESET_L OUT	19 28
19 16 OUT	SOC_UART_R2D	AC2	GPP_C13/UART1_TXD/ISH_UART1_TXD		W10	GPP_G5/SD_CD*	TBT_T_PCI_RESET_L OUT	70
19 16 OUT	SOC_UART_RTS_L	AC3	GPP_C14/UART1_RTS*/ISH_UART1_RTS*		AY8	GPP_A18/ISH_GP0	SPIROM_USE_MLB OUT	16 47 72
19 16 IN	SOC_UART_CTS_L	AB4	GPP_C15/UART1_CTS*/ISH_UART1_CTS*		BA8	GPP_A19/ISH_GP1	LCD_IRQ_L OUT	16 66 72
67 19 IN	SSD_RESET_L	N11	GPP_E22		BB7	GPP_A20/ISH_GP2	TBT_X_DPMUX_SEL IN	70
28 16 OUT	TBT_POC_RESET	N12	GPP_E23		BA7	GPP_A21/ISH_GP3	TBT_T_DPMUX_SEL IN	70
70	TP_BT_I2S_CLK	AK6	GPP_F0/I2S2_SCLK		AY7	GPP_A22/ISH_GP4	TPAD_SPI_IF_EN OUT	16 38 72
70	TP_BT_I2S_SYNC	AK7	GPP_F1/I2S2_SFRM	(1.8V)	AW7	GPP_A23/ISH_GP5	TPAD_SPI_INT_L IN	16 38 72
70	TP_BT_I2S_R2D	AK9	GPP_F2/I2S2_TXD		AP13	SX_EXIT_HOLDOFF*/GPP_A12/BM_BUSY*/ISH_GP6	AUD_PWR_EN OUT	16 19 49
70	TP_BT_I2S_D2R	AK10	GPP_F3/I2S2_RXD					

=PP3V3_S0_PCH 5 13 14 19 60 69

=PP3V3_SUS_PCH_VCCPGPPA 8 13 14 15 69

R1643	47K	5%	1/20W	MF	201	SOC_UART_D2R	16 19
R1642	47K	5%	1/20W	MF	201	SOC_UART_R2D	16 19
R1641	47K	5%	1/20W	MF	201	SOC_UART_RTS_L	16 19
R1640	47K	5%	1/20W	MF	201	SOC_UART_CTS_L	16 19
R1650	100K	5%	1/20W	MF	201	SPIROM_USE_MLB	16 47 72
R1652	100K	5%	1/20W	MF	201	AUD_PWR_EN:S0 AUD_PWR_EN	16 19 49
R1653	47K	5%	1/20W	MF	201	AUD_SPI_CS_L	16 19
R1654	47K	5%	1/20W	MF	201	AUD_SPI_CLK	16 19
R1655	47K	5%	1/20W	MF	201	AUD_SPI_MISO	16 19
R1656	1K	5%	1/20W	MF	201	AUD_SPI_MOSI	16 19
R1657	47K	5%	1/20W	MF	201	TPAD_SPI_CS_L	16 38
R1658	47K	5%	1/20W	MF	201	TPAD_SPI_CLK	16 38 72
R1659	47K	5%	1/20W	MF	201	TPAD_SPI_MISO	16 38 72
R1660	150K	5%	1/20W	MF	201	TPAD_SPI_MOSI	16 38 72
R1674	100K	5%	1/20W	MF	201	TPAD_SPI_INT_L	16 38 72
R1673	100K	5%	1/20W	MF	201	TPAD_SPI_IF_EN	16 38 72
R1661	47K	5%	1/20W	MF	201	PCH_BT_UART_D2R	16 35
R1662	47K	5%	1/20W	MF	201	PCH_BT_UART_R2D	16 35
R1663	47K	5%	1/20W	MF	201	PCH_BT_UART_RTS_L	16 35
R1664	47K	5%	1/20W	MF	201	PCH_BT_UART_CTS_L	16 35
R1665	100K	5%	1/20W	MF	201	AP_S0IX_WAKE_SEL	16 18
R1666	100K	5%	1/20W	MF	201	AP_S0IX_WAKE_L	16 18
R1667	100K	5%	1/20W	MF	201	AP_DEV_WAKE	16 34 35
R1669	100K	5%	1/20W	MF	201	LCD_IRQ_L DRIVEN PUSH PULL FROM SWITCHED RAIL.	16 66 72
R1668	100K	5%	1/20W	MF	201	TBT_X_PLUG_EVENT_L	16 28
R1671	100K	5%	1/20W	MF	201	TBT_T_PLUG_EVENT_L	16 19
R1672	100K	5%	1/20W	MF	201	TBT_POC_RESET	16 28

MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

16 MLB_BOARD_ID0
16 MLB_BOARD_ID1
16 MLB_BOARD_ID2
16 MLB_BOARD_ID3
16 MLB_BOARD_ID4

OMIT_TABLE	OMIT_TABLE	OMIT_TABLE	OMIT_TABLE	OMIT_TABLE
R1694	R1693	R1692	R1691	R1690
1K 5% 1/20W MF 201	1K 5% 1/20W MF 201	1K 5% 1/20W MF 201	1K 5% 1/20W MF 201	1K 5% 1/20W MF 201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>

BOM_COST_GROUP=CPU & CHIPSET

合肥怡飞苹果维修qq：82669515
qq群：241000

DESIGN: X502/MLB CATZ
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PAGE TITLE
PCH SPI/UART/GPIO

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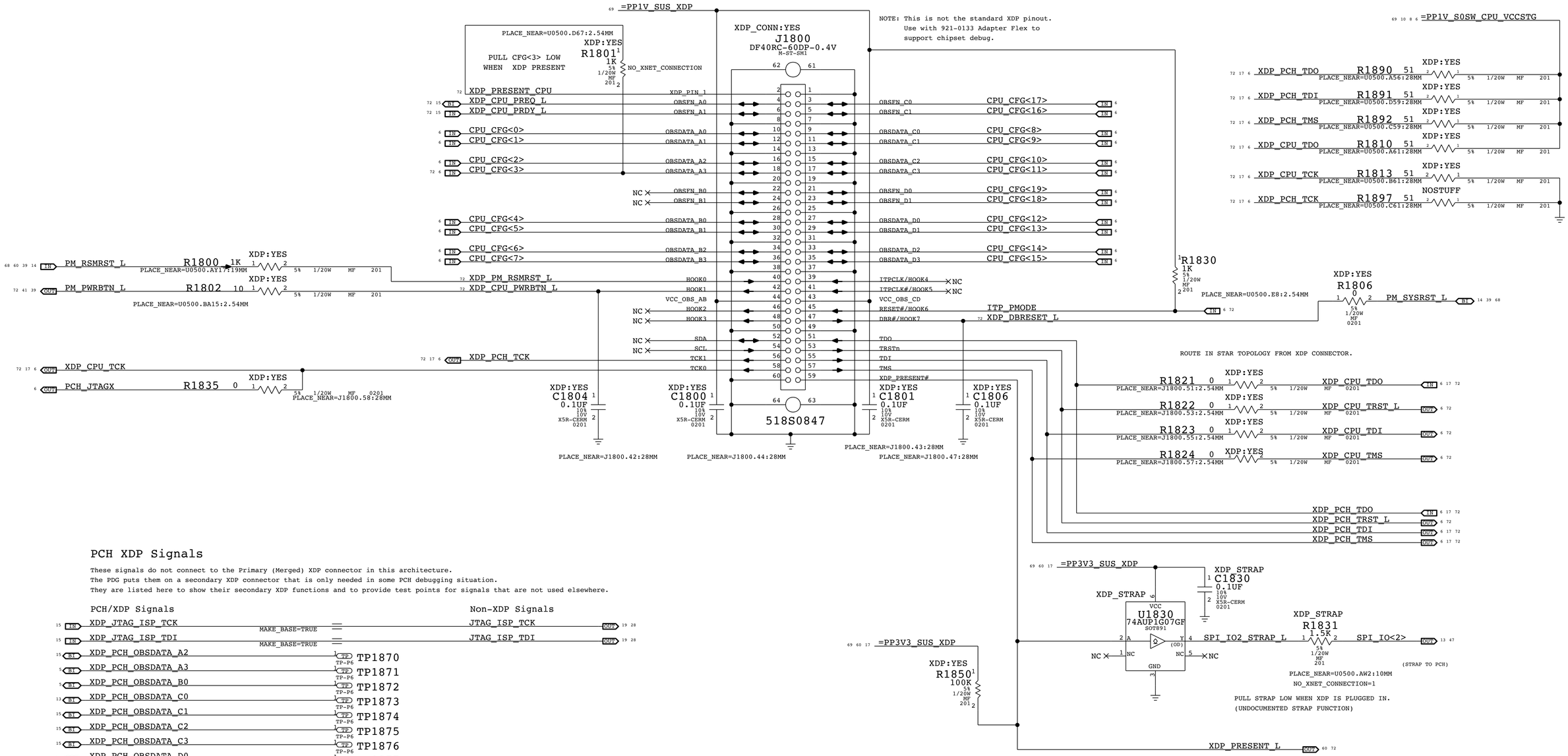
Primary / Merged (CPU/PCH) Micro2-XDP



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals			Non-XDP Signals
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE		JTAG_ISP_TCK
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE		JTAG_ISP_TDI
XDP_PCH_OBSDATA_A2		TP1870	
XDP_PCH_OBSDATA_A3		TP1871	
XDP_PCH_OBSDATA_B0		TP1872	
XDP_PCH_OBSDATA_C0		TP1873	
XDP_PCH_OBSDATA_C1		TP1874	
XDP_PCH_OBSDATA_C2		TP1875	
XDP_PCH_OBSDATA_C3		TP1876	
XDP_PCH_OBSDATA_D0		TP1877	
XDP_PCH_OBSDATA_D1		TP1878	
XDP_PCH_OBSDATA_D2		TP1879	
XDP_PCH_OBSDATA_D3		TP1880	
XDP_PCH_OBSFN_C1		TP1881	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE		USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE		USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE		USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE		USB_EXTD_OC_L

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=DEBUG

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CPU/PCH Merged XDP

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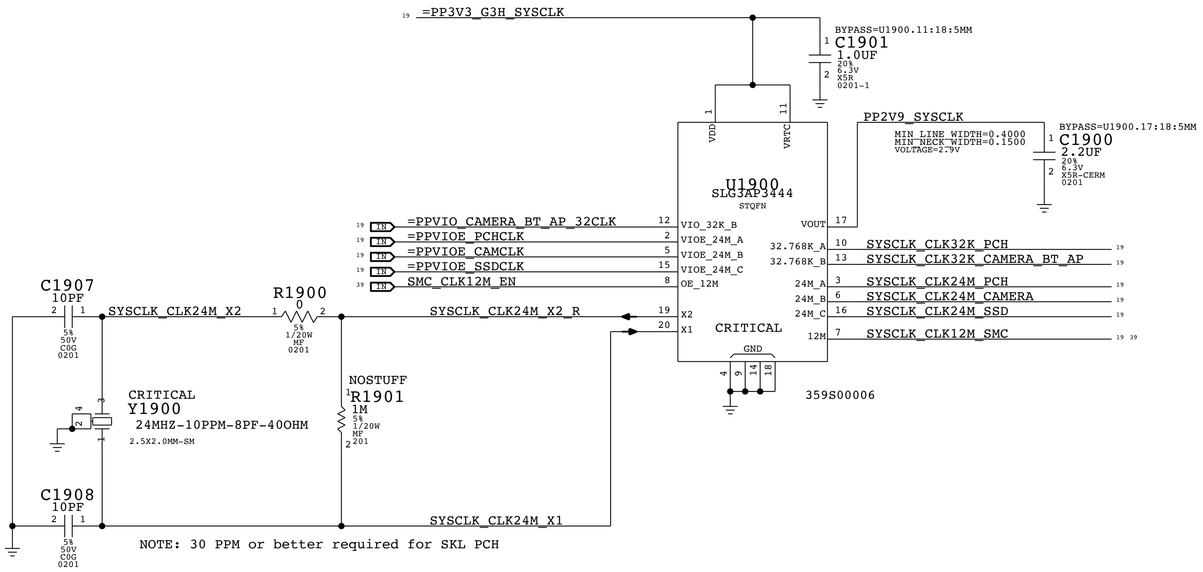
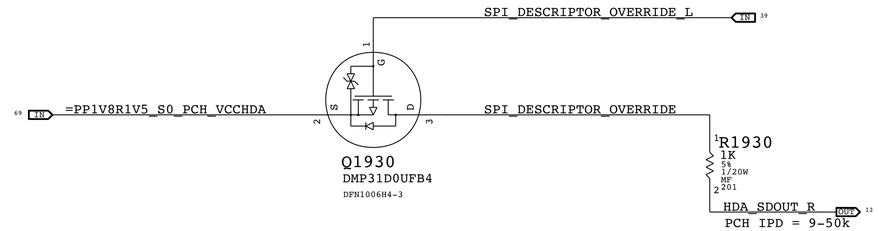
System 32kHz / 12MHz / 24MHz Clock Generator

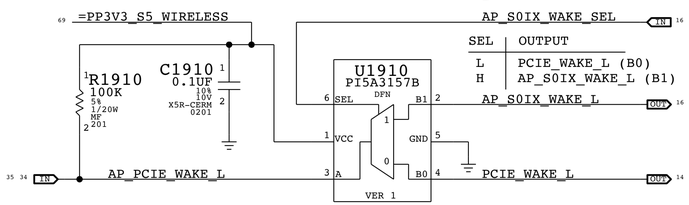


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

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qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 1

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D

REVISION: 1.0.0

BRANCH

PAGE: 19 OF 500

SHEET: 18 OF 73

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OPTION STRAPS

PROJECT DEPENDANT

STUFF PULL-UPS TO ENABLE INTERNAL GPU DP PORTS.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWNS TO DISABLE.

=PP3V3_S0_PCH 5 13 14 16 19 60 69

R2020 2.2K 5% 1/20W MF 201 — IG_DDI1_EN (STRAP-OPTION) — PCH_DDPB_CTRLDATA 13
R2021 2.2K 5% 1/20W MF 201 — IG_DDI2_EN (STRAP-OPTION) — PCH_DDPC_CTRLDATA 13

STUFF PULL-UP TO ENABLE BSSB (DCI) CLK/DI ON GPP_D11, _D12.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWN FOR BSSB ON USB-SS.

=PP3V3_SUS_PCH_VCCPGPPB 8 12 69

R2022 1K 5% 1/20W MF 201 — BSSB_ON_GPIOS (STRAP-OPTION) — PCH_STRP_BSSB_SEL_GPIO 13

GREENCLK CLOCK CONNECTIONS.

10 =PP3V3_G3H_SYSCLK — PP3V3_G3H 28 41 42 47 51 52 53 60 68 69 72

19 18 =PPVIO_CAMERA_BT_AP_32CLK — PPVIO_BT_AP_32CLK (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800) — =PP3V3_S4_WLAN 34 69

BT_CLK32K:YES
R2030 0 5% 1/20W MF 0201

BT_CLK32K:NO
R2031[1] 100K 5% 1/20W MF 201

18 =PPVIOE_SSDCLK — PD_PPVIOE_SSDCLK (MAKE_BASE=TRUE) — XW2000 SM

19 18 =PPVIOE_CAMCLK — PPVIOE_CAMCLK (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800) — =PPVDDIO_S0_CAMCLK 36

XW2002 SM

PCH 24MHz VIOE Options

72 69 64 63 62 PP1V_S5G — XW2065 SM — PP1V_S5G_PCHCLK (VOLTAGE=1V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800) — R2065 0 5% 1/20W MP 0201 — =PPVIOE_PCHCLK 18 19

PP1V_SUSRS0SW_PCHCLK (VOLTAGE=1V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800; MAKE_BASE=TRUE)

PCH24M:SUS

PCH24M:S0SW
PP1V_S0SW_PCHCLK (VOLTAGE=1V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800) — R2066 0 5% 1/20W MP 0201

PCH24M:S0SW
PM_SLP_S0S3_L — IN 60 68 72

SYM VER 3
DFN1006H4-3
DMN32D2LFB4
Q2065
CRITICAL

19 18 =PPVIO_CAMERA_BT_AP_32CLK 18 19
=PPVIOE_PCHCLK 18 19
=PPVIOE_CAMCLK 18 19

BYPASS=U1900.12:18:5MM
BYPASS=U1900.02:18:5MM
BYPASS=U1900.05:18:5MM

C2004 0.1UF 10% 10V X5R-CERM 0201
C2005 0.1UF 10% 10V X5R-CERM 0201
C2006 0.1UF 10% 10V X5R-CERM 0201

18 IN SYSCLK_CLK32K_PCH — PCH_CLK32K_RTCX1 OUT 15
70 (MAKE_BASE=TRUE; MAKE_BASE=TRUE) TP_PCH_CLK32K_RTCX2 — PCH_CLK32K_RTCX2 IN 15

BT_CLK32K:YES
R2032 0 5% 1/20W MP 0201

18 IN SYSCLK_CLK32K_CAMERA_BT_AP — SYSCLK_CLK32K_BT_AP OUT 34
SYSCLK_CLK32K_BT_AP_R (MAKE_BASE=TRUE)

18 IN SYSCLK_CLK24M_PCH — PCH_CLK24M_XTALIN OUT 15
70 (MAKE_BASE=TRUE; MAKE_BASE=TRUE) TP_PCH_CLK24M_XTALOUT — PCH_CLK24M_XTALOUT IN 15

18 IN SYSCLK_CLK24M_SSD — TP_SYSCLK_CLK24M_SSD (MAKE_BASE=TRUE) 70

18 IN SYSCLK_CLK24M_CAMERA — CLK25M_CAM_CLKP (MAKE_BASE=TRUE) OUT 36

39 18 IN SYSCLK_CLK12M_SMC OUT

=PP3V3_S0_PCH 5 13 14 16 19 60 69

R2071 47K 5% 1/20W MF 201 — SSD_CLKREQ_L 19 67
R2072 47K 5% 1/20W MF 201 — TBT_X_CLKREQ_L 19 26
R2074 47K 5% 1/20W MF 201 — AP_CLKREQ_L 19 34 35
R2075 47K 5% 1/20W MF 201 — CAMERA_CLKREQ_L 19 36

SERIES R FOR VOLTAGE DIVIDER WHEN PCH IS DRIVING IN L1 SUB-STATE.

15 OUT =SSD_CLKREQ_L — SSD_CLKREQ_R_L (MAKE_BASE=TRUE) — R2001 1K 1/20W 5% 201 MF — SSD_CLKREQ_L IN 19 67
15 OUT =AP_CLKREQ_L — AP_CLKREQ_R_L (MAKE_BASE=TRUE) — R2002 1K 1/20W 5% 201 MF — AP_CLKREQ_L IN 19 34 35
15 OUT =CAMERA_CLKREQ_L — CAMERA_CLKREQ_R_L (MAKE_BASE=TRUE) — R2003 1K 1/20W 5% 201 MF — CAMERA_CLKREQ_L IN 19 36
15 OUT =TBT_X_CLKREQ_L — TBT_X_CLKREQ_R_L (MAKE_BASE=TRUE) — R2004 1K 1/20W 5% 201 MF — TBT_X_CLKREQ_L IN 19 26

UNUSED PCH XDP SIGNALS NEED TEST POINTS.

28 17 IN JTAG_ISP_TCK — TP2070 (TP-P6)
28 17 IN JTAG_ISP_TDI — TP2071 (TP-P6)
17 IN USB_EXTD_OC_L — TP2072 (TP-P6)
17 IN USB_EXTC_OC_L — TP2073 (TP-P6)

EXTRA BPM TESTPOINTS

6 IN XDP_BPM_L<1> — (MAKE_BASE=TRUE) — TP_XDP_BPM_L<1> 70
6 IN XDP_BPM_L<2> — (MAKE_BASE=TRUE) — TP_XDP_BPM_L<2> 70
6 IN XDP_BPM_L<3> — (MAKE_BASE=TRUE) — TP_XDP_BPM_L<3> 70

IFDIM TRIGGERS USING R2055 & R2056 PADS
ASK DC/DC GROUP FOR DETAILS.

6 IN XDP_BPM_L<0> — NOSTUFF R2055 100K 5% 1/16W MF-LF 402
6 IN TP_CPU_RSVD_AK13 — (MAKE_BASE=TRUE) — CPU_RSVD_AK13 — NOSTUFF R2056 100K 5% 1/16W MF-LF 402

UNUSED GPIO SIGNALS

16 IN SOC_UART_D2R — (MAKE_BASE=TRUE) — PU_SOC_UART_D2R
16 IN SOC_UART_R2D — (MAKE_BASE=TRUE) — PU_SOC_UART_R2D
16 IN SOC_UART_RTS_L — (MAKE_BASE=TRUE) — PU_SOC_UART_RTS_L
16 IN SOC_UART_CTS_L — (MAKE_BASE=TRUE) — PD_SOC_UART_CTS_L
16 IN TBT_T_PLUG_EVENT_L — (MAKE_BASE=TRUE) — PU_TBT_T_PLUG_EVENT_L
14 IN PCH_SWD_CLK — (MAKE_BASE=TRUE) — PU_PCH_SWD_CLK
14 BI PCH_SWD_IO — (MAKE_BASE=TRUE) — PU_PCH_SWD_IO
14 IN PCH_SWD_MUX_SEL — (MAKE_BASE=TRUE) — PD_PCH_SWD_MUX_SEL
13 IN LCD_PSR_EN — (MAKE_BASE=TRUE) — PD_LCD_PSR_EN
16 IN AUD_SPI_CS_L — (MAKE_BASE=TRUE) — PU_AUD_SPI_CS_L
16 IN AUD_SPI_CLK — (MAKE_BASE=TRUE) — PD_AUD_SPI_CLK
16 OUT AUD_SPI_MISO — (MAKE_BASE=TRUE) — PD_AUD_SPI_MISO
16 IN AUD_SPI_MOSI — (MAKE_BASE=TRUE) — PU_AUD_SPI_MOSI
15 OUT SPKR_ID0 — (MAKE_BASE=TRUE) — TP_SPKR_ID0 70
16 OUT SPKR_ID1 — (MAKE_BASE=TRUE) — TP_SPKR_ID1

13 IN CAMERA_PWR_EN_PCH — R2060 0 5% 1/20W MF 0201 — CAMERA_PWR_EN OUT 13 19 36

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qq群： 241000

69 59 54 14 10 8 6 =PP1V_S3_CPU_VCCST — R2061 51 5% 1/20W MP 201 — CPU_CATERR_L 68 39 6 OUT

14 IN SOC_S2R_L — (MAKE_BASE=TRUE) — SOC_WAKE_L

69 60 19 16 14 13 5 =PP3V3_S0_PCH
C2040 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
U2040
74LVC1G08
SOT891

60 14 IN PM_PCH_PWROK — 1 — 2 — 6 — 4 — PM_PCH_PWROK_BUF
5 — 3 — NC

R2040 100K 5% 1/20W MF 201 — AUD_PWR_EN 16 49
R2041 100K 5% 1/20W MF 201 — CAMERA_PWR_EN 13 19 36

BOM_COST_GROUP=CPU & CHIPSET

RESETS

68 35 14 IN PLT_RST_L

R2014[1] 470K 5% 1/20W MF 201

R2010 100K 5% 1/20W MF 201 — CAMERA_RESET_L OUT 13 36
R2011 100K 5% 1/20W MF 201 — AP_RESET_L OUT 16 34 35
R2012 100K 5% 1/20W MF 201 — SSD_RESET_L OUT 16 67
R2013 100K 5% 1/20W MF 201 — TBT_X_PCI_RESET_L OUT 16 19 28
R2015 33 5% 1/20W MF 201 — SMC_LRESET_L OUT 39

26 PM_PLT_RST_TBT_X_L — (MAKE_BASE=TRUE) — TBT_X_PCI_RESET_L 16 19 28

S3X SSD CONTROL

PCH — S3X SSD DOWN

60 OUT SSD_PWR_REQ — (MAKE_BASE=TRUE) — STORAGE_LATCH IN 67

UNUSED GPIO SIGNALS

13 IN SOC_ALS_UART_R2D — (MAKE_BASE=TRUE) — PU_SSD_UART_R2D
13 OUT SOC_ALS_UART_D2R — (MAKE_BASE=TRUE) — PU_SSD_UART_D2R
13 IN PCH_UART2_CTS_L — (MAKE_BASE=TRUE) — PD_SSD_UART_CTS_L

PROBE POINTS

28 15 IN PCIE_TBT_X_R2D_C_P<0>
28 15 IN PCIE_TBT_X_R2D_C_N<0>

NO_XNET_CONNECTION=1
NOSTUFF
PLACE_NEAR=C3040.1:1MM
C2090 0.22UF 20% 2.5V X5R 0201 — TBTXR2DP0 (PLACE_NEAR=C2090.2:1MM) — R2090 51 5% 1/20W MP 201 — NOSTUFF
C2091 0.22UF 20% 2.5V X5R 0201 — TBTXR2DN0 (PLACE_NEAR=C3040.1:1MM) — R2091 51 5% 1/20W MP 201 — NOSTUFF

28 26 OUT DP_X_SNK1_ML_C_P<0>
28 26 IN DP_X_SNK1_ML_C_N<0>

NO_XNET_CONNECTION=1
NOSTUFF
PLACE_NEAR=C3040.1:1MM
C2092 0.1UF 10% 16V X5R-CERM 0201 — DPX1P0 (PLACE_NEAR=C2090.2:6MM) — R2092 51 5% 1/20W MP 201 — NOSTUFF
C2093 0.1UF 10% 16V X5R-CERM 0201 — DPX1N0 (PLACE_NEAR=C2090.2:5MM) — R2093 51 5% 1/20W MP 201 — NOSTUFF

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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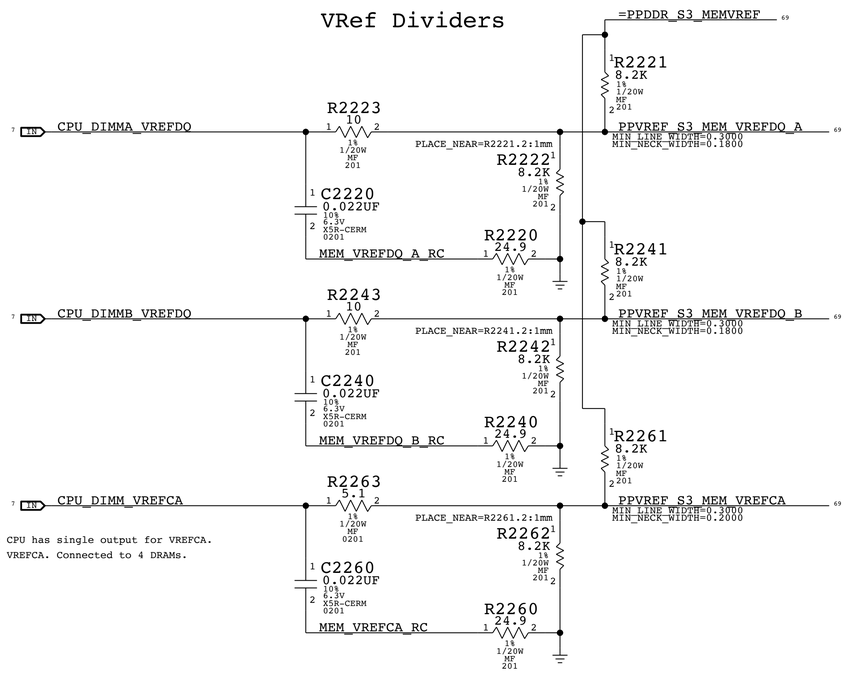
CPU-Based Margining

VRef Dividers



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

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qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 VREF Margining

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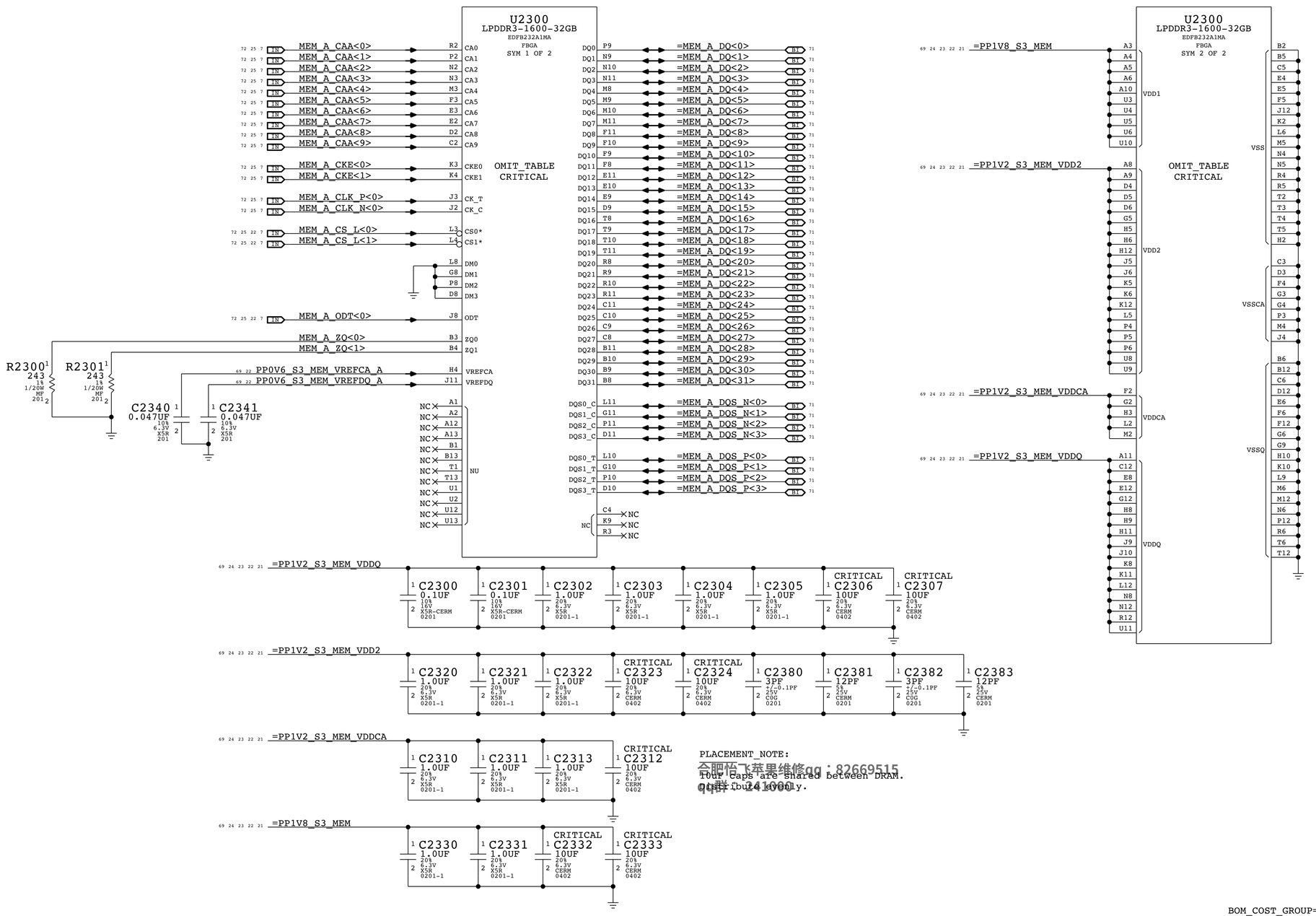
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:
four caps are shared between DRAM.
Place 1pu only.

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qq群：241000

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel A (00-31)
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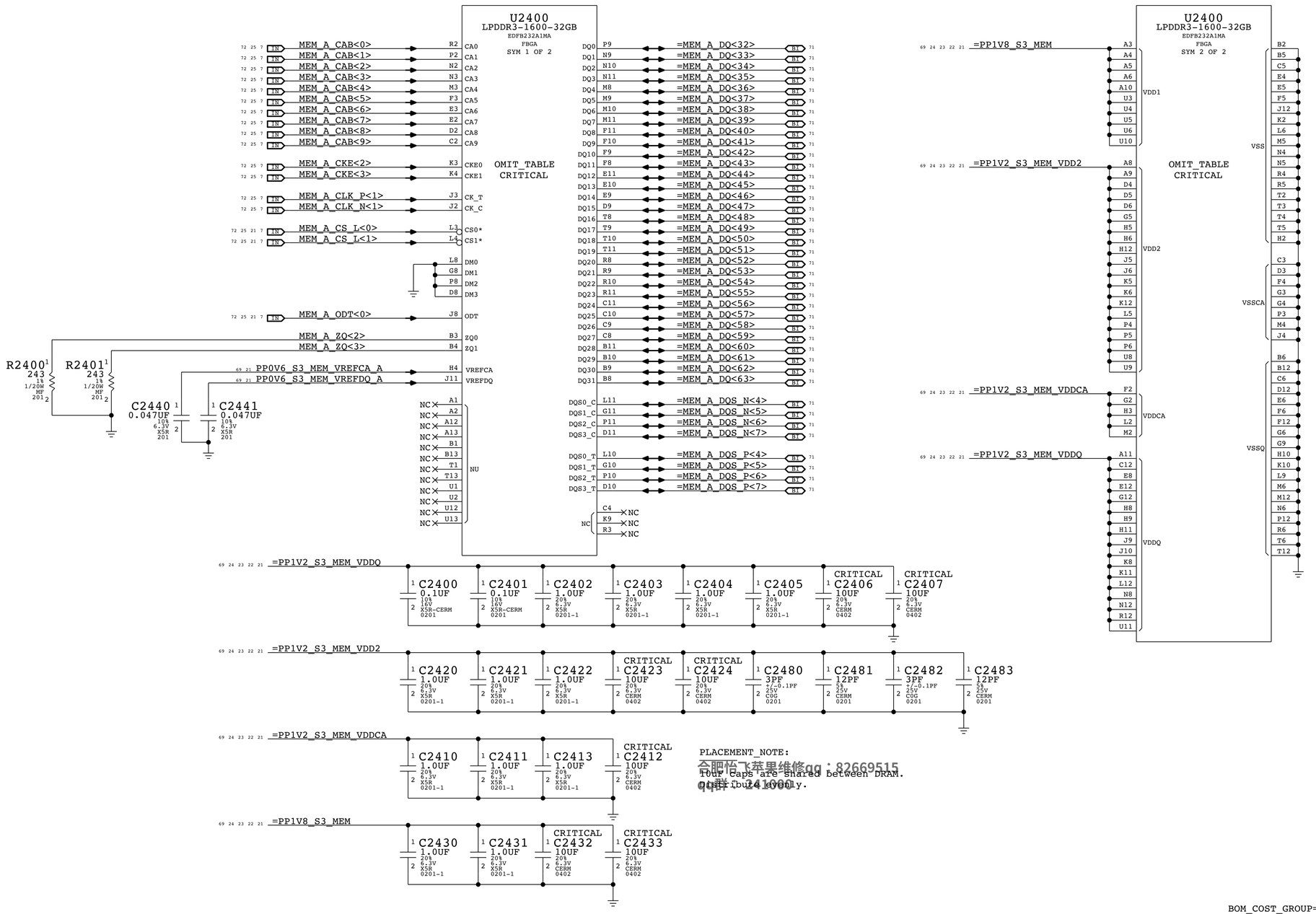
LPDDR3 CHANNEL A (32-63)



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qq群：241000

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
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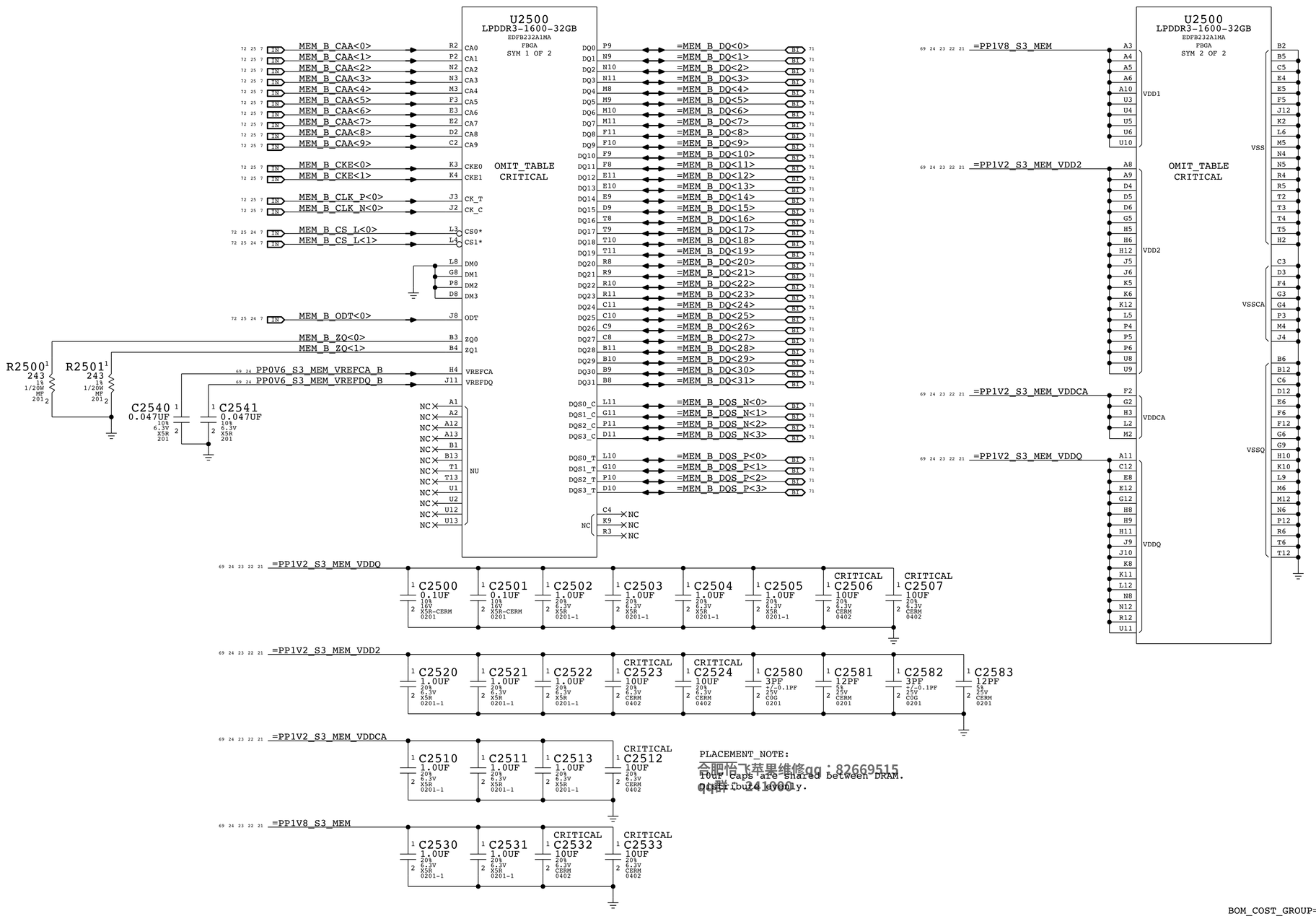
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:
four caps are shared between DRAM.
put them only.

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qq群：241000

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
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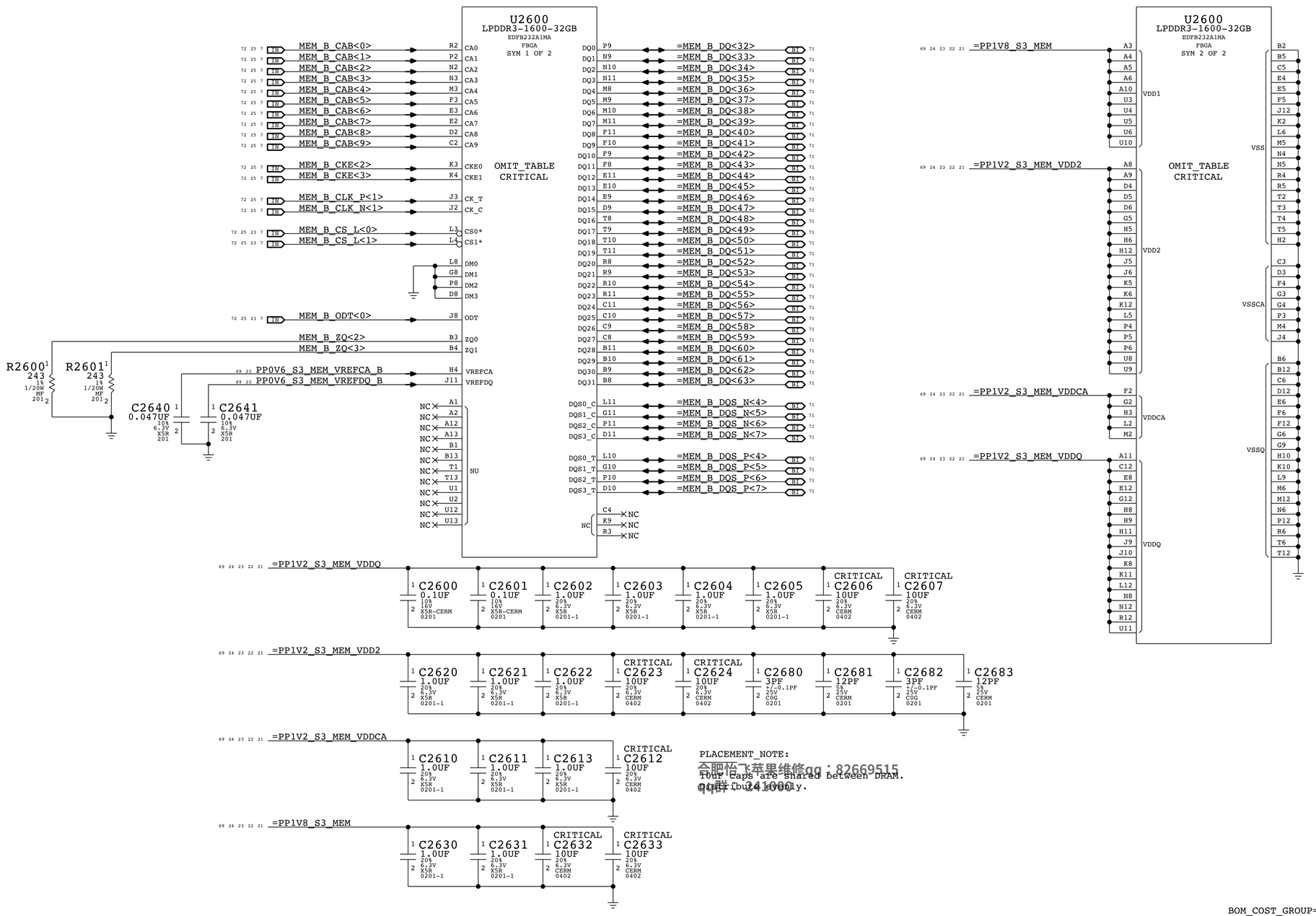
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:
Four caps are shared between DRAM.
Place four only.

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电话：241000

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
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Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

69 =PP0V6_S0_MEM_VTT_A

72 21 7	IN	MEM_A_CAA<9>	R2700	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<8>	R2701	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<6>	R2702	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<7>	R2703	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<5>	R2704	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CLK_P<0>	R2705	39	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CLK_N<0>	R2706	39	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CKE<1>	R2707	82	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CKE<0>	R2708	82	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<4>	R2709	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<3>	R2710	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<2>	R2711	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<1>	R2712	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<0>	R2713	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<9>	R2714	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<8>	R2715	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<6>	R2716	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<7>	R2717	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<5>	R2718	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CLK_P<1>	R2719	39	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CLK_N<1>	R2720	39	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CKE<2>	R2721	82	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CKE<3>	R2722	82	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<4>	R2723	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<2>	R2724	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<3>	R2725	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<1>	R2726	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<0>	R2727	68	1%	1/20W	201	MF	
72 22 21 7	IN	MEM_A_CS_L<0>	R2728	82	1%	1/20W	201	MF	
72 22 21 7	IN	MEM_A_CS_L<1>	R2729	82	1%	1/20W	201	MF	
72 22 21 7	IN	MEM_A_ODT<0>	R2730	82	1%	1/20W	201	MF	

C2700	0.47UF	20%	4V	CERM-X5R-1	201
C2730	12PF	5%	25V	CERM	0201
C2701	0.47UF	20%	4V	CERM-X5R-1	201
C2702	0.47UF	20%	4V	CERM-X5R-1	201
C2703	0.47UF	20%	4V	CERM-X5R-1	201
C2704	0.47UF	20%	4V	CERM-X5R-1	201
C2705	0.47UF	20%	4V	CERM-X5R-1	201
C2706	0.47UF	20%	4V	CERM-X5R-1	201
C2707	0.47UF	20%	4V	CERM-X5R-1	201
C2708	0.47UF	20%	4V	CERM-X5R-1	201
C2709	0.47UF	20%	4V	CERM-X5R-1	201
C2722	3PF	+/-0.1PF	25V	C0G	0201
CRITICAL C2720	20UF	20%	6.3V	CERM-X5R	0402
NOSTUFF CRITICAL C2721	20UF	20%	6.3V	CERM-X5R	0402

69 =PP0V6_S0_MEM_VTT_B

72 23 7	IN	MEM_B_CAA<9>	R2740	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<8>	R2741	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<7>	R2742	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<6>	R2743	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<5>	R2744	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CLK_P<0>	R2745	39	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CLK_N<0>	R2746	39	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CKE<1>	R2747	82	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CKE<0>	R2748	82	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<4>	R2749	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<2>	R2750	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<3>	R2751	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<1>	R2752	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<0>	R2753	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<9>	R2754	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<8>	R2755	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<7>	R2756	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<6>	R2757	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<5>	R2758	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CLK_N<1>	R2759	39	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CLK_P<1>	R2760	39	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CKE<2>	R2761	82	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CKE<3>	R2762	82	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<4>	R2763	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<2>	R2764	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<3>	R2765	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<1>	R2766	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<0>	R2767	68	1%	1/20W	201	MF	
72 24 23 7	IN	MEM_B_CS_L<0>	R2768	82	1%	1/20W	201	MF	
72 24 23 7	IN	MEM_B_CS_L<1>	R2769	82	1%	1/20W	201	MF	
72 24 23 7	IN	MEM_B_ODT<0>	R2770	82	1%	1/20W	201	MF	

C2710	0.47UF	20%	4V	CERM-X5R-1	201
C2731	12PF	5%	25V	CERM	0201
C2711	0.47UF	20%	4V	CERM-X5R-1	201
C2712	0.47UF	20%	4V	CERM-X5R-1	201
C2713	0.47UF	20%	4V	CERM-X5R-1	201
C2714	0.47UF	20%	4V	CERM-X5R-1	201
C2715	0.47UF	20%	4V	CERM-X5R-1	201
C2716	0.47UF	20%	4V	CERM-X5R-1	201
C2717	0.47UF	20%	4V	CERM-X5R-1	201
C2718	0.47UF	20%	4V	CERM-X5R-1	201
C2719	0.47UF	20%	4V	CERM-X5R-1	201
C2742	3PF	+/-0.1PF	25V	C0G	0201
CRITICAL C2740	20UF	20%	6.3V	CERM-X5R	0402
NOSTUFF CRITICAL C2741	20UF	20%	6.3V	CERM-X5R	0402

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BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

REVISION 1.0.0

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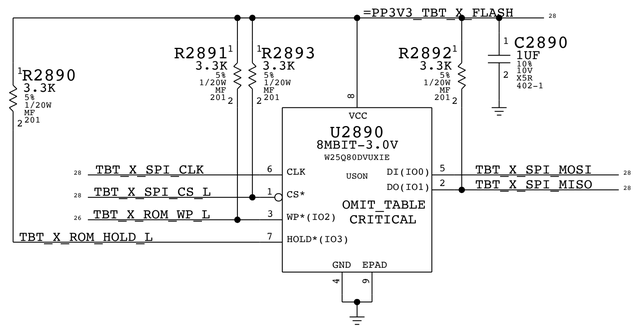


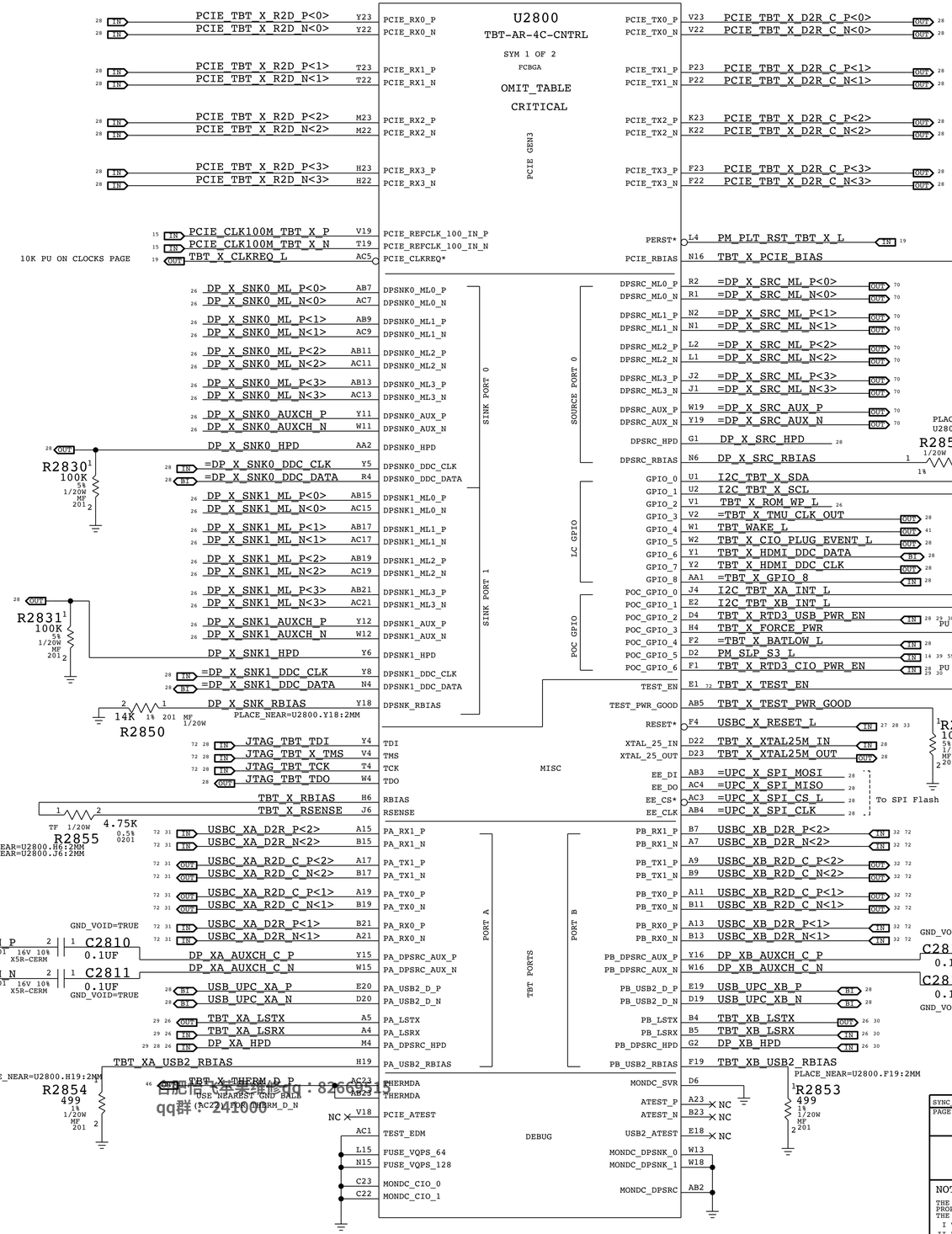
SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_P<0>
DP_X_SNK0_ML_C_N<0>	C2821	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_N<0>
DP_X_SNK0_ML_C_P<1>	C2822	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_P<1>
DP_X_SNK0_ML_C_N<1>	C2823	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_N<1>
DP_X_SNK0_ML_C_P<2>	C2824	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_P<2>
DP_X_SNK0_ML_C_N<2>	C2825	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_N<2>
DP_X_SNK0_ML_C_P<3>	C2826	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_P<3>
DP_X_SNK0_ML_C_N<3>	C2827	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_ML_N<3>
DP_X_SNK0_AUXCH_C_P	C2828	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_AUXCH_P
DP_X_SNK0_AUXCH_C_N	C2829	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK0_AUXCH_N

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_P<0>
DP_X_SNK1_ML_C_N<0>	C2831	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_N<0>
DP_X_SNK1_ML_C_P<1>	C2832	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_P<1>
DP_X_SNK1_ML_C_N<1>	C2833	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_N<1>
DP_X_SNK1_ML_C_P<2>	C2834	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_P<2>
DP_X_SNK1_ML_C_N<2>	C2835	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_N<2>
DP_X_SNK1_ML_C_P<3>	C2836	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_P<3>
DP_X_SNK1_ML_C_N<3>	C2837	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_ML_N<3>
DP_X_SNK1_AUXCH_C_P	C2838	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_AUXCH_P
DP_X_SNK1_AUXCH_C_N	C2839	0.1UF	10% 16V X5R-CERM 0201	DP_X_SNK1_AUXCH_N

R2862	DP_XA_HPD	100K 5% 1/20W MF 201
R2872	DP_XB_HPD	100K 5% 1/20W MF 201
R2860	TBT_XA_LSTX	1M 5% 1/20W MF 201
R2861	TBT_XA_LSRX	1M 5% 1/20W MF 201
R2870	TBT_XB_LSTX	1M 5% 1/20W MF 201
R2871	TBT_XB_LSRX	1M 5% 1/20W MF 201



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SYNC_MASTER=X362 SYNC_DATE=07/29/2015

PAGE TITLE

USB-C HIGH SPEED 1

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

REVISION 1.0.0

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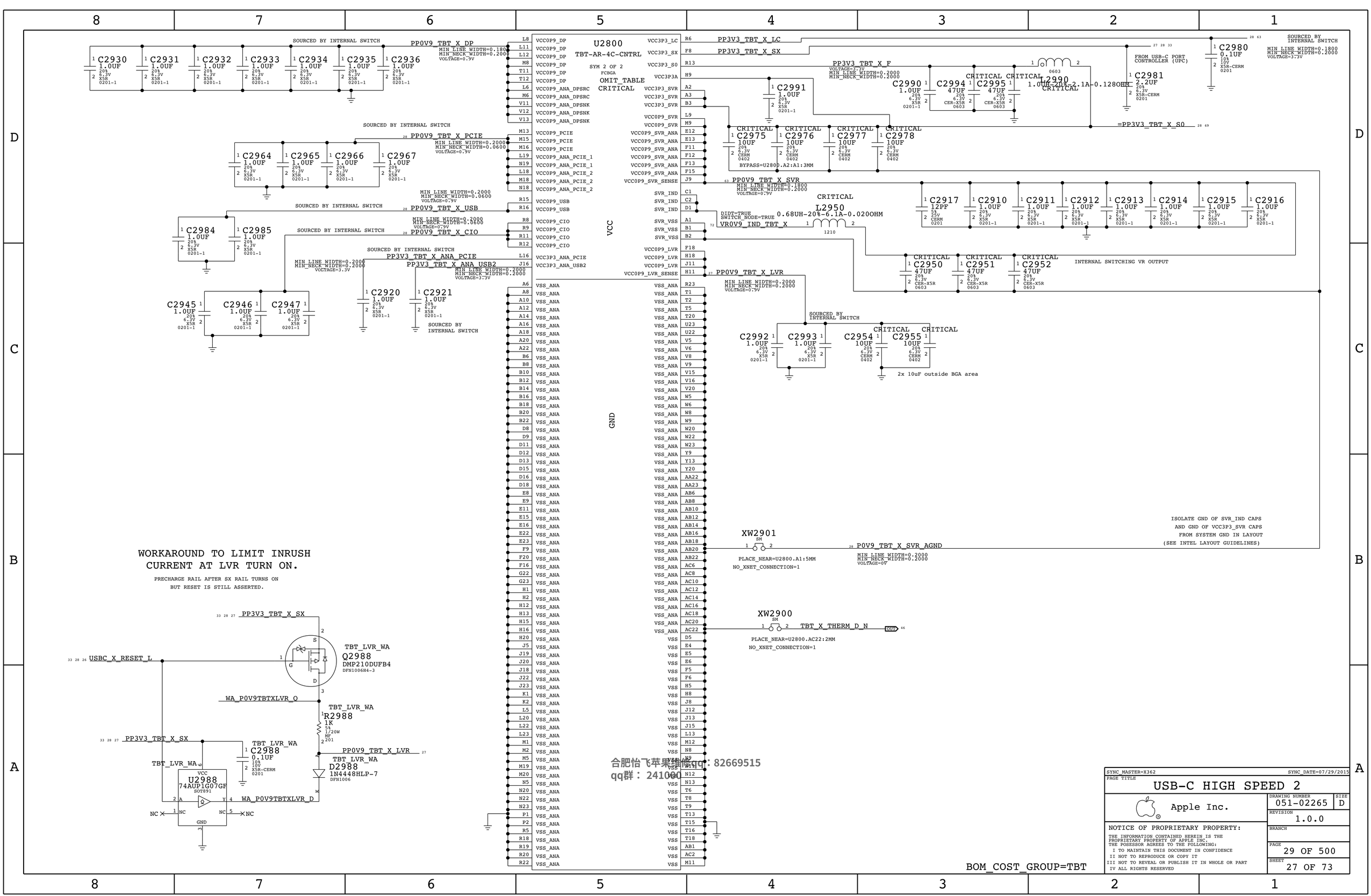

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RIDGE AC COUPLING

R2D

PCIE_TBT_X_R2D_C_P<0>	C3040	0.22UF	PCIE_TBT_X_R2D_P<0>	
PCIE_TBT_X_R2D_C_N<0>	C3041	0.22UF	PCIE_TBT_X_R2D_N<0>	
PCIE_TBT_X_R2D_C_P<1>	C3042	0.22UF	PCIE_TBT_X_R2D_P<1>	
PCIE_TBT_X_R2D_C_N<1>	C3043	0.22UF	PCIE_TBT_X_R2D_N<1>	
PCIE_TBT_X_R2D_C_P<2>	C3044	0.22UF	PCIE_TBT_X_R2D_P<2>	TBT_PCIE_4LANES
PCIE_TBT_X_R2D_C_N<2>	C3045	0.22UF	PCIE_TBT_X_R2D_N<2>	TBT_PCIE_4LANES
PCIE_TBT_X_R2D_C_P<3>	C3046	0.22UF	PCIE_TBT_X_R2D_P<3>	TBT_PCIE_4LANES
PCIE_TBT_X_R2D_C_N<3>	C3047	0.22UF	PCIE_TBT_X_R2D_N<3>	TBT_PCIE_4LANES

D2R

PCIE_TBT_X_D2R_C_P<0>	C3050	0.22UF	PCIE_TBT_X_D2R_P<0>	
PCIE_TBT_X_D2R_C_N<0>	C3051	0.22UF	PCIE_TBT_X_D2R_N<0>	
PCIE_TBT_X_D2R_C_P<1>	C3052	0.22UF	PCIE_TBT_X_D2R_P<1>	
PCIE_TBT_X_D2R_C_N<1>	C3053	0.22UF	PCIE_TBT_X_D2R_N<1>	
PCIE_TBT_X_D2R_C_P<2>	C3055	0.22UF	PCIE_TBT_X_D2R_P<2>	TBT_PCIE_4LANES
PCIE_TBT_X_D2R_C_N<2>	C3056	0.22UF	PCIE_TBT_X_D2R_N<2>	TBT_PCIE_4LANES
PCIE_TBT_X_D2R_C_P<3>	C3057	0.22UF	PCIE_TBT_X_D2R_P<3>	TBT_PCIE_4LANES
PCIE_TBT_X_D2R_C_N<3>	C3054	0.22UF	PCIE_TBT_X_D2R_N<3>	TBT_PCIE_4LANES

ACE RPD STRAPPING

CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE

USBC_XA_RPD_G1	R3026	0	USBC_XA_CC1
USBC_XA_RPD_G2	R3022	0	USBC_XA_CC2
USBC_XB_RPD_G1	R3011	0	USBC_XB_CC1
USBC_XB_RPD_G2	R3024	0	USBC_XB_CC2

ACE BUSPOWERZ STRAPPING

R3017	0	UPC_XA_BUSPOWERZ
R3019	0	UPC_XB_BUSPOWERZ

PU BUSPOWERZ TO LDO_3V3 TO NOT PASS VBUS TO SYS UNDER DB CASE

PU BUSPOWERZ TO 1V8D TO PASS VBUS TO SYS UNDER DB CASE USES INT POWER PATH

GND BUSPOWERZ TO PASS VBUS TO SYS UNDER DB CASE USES EXT POWER PATH

RIDGE DEBUG CONN

J3099 505070-1220 M-ST-SM UPC_DBG_HDR

TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
ARKANOID_P5	5	6	PP3V3_TBT_X_SX
ARKANOID_P7	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO
	15	16	

516S00115

ACE DEBUG CONN

J3098 505070-1220 M-ST-SM UPC_DBG_HDR

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
=I2C_UPC_XA_SCL2	3	4	I2C_TBT_X_SDA
=I2C_UPC_XA_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX
	15	16	

516S00115

DP_X_SNK1_HPD	ARKANOID:HPD	R3080	ARKANOID_P5
SMC_DEBUGPRT_RX_L	ARKANOID:MOJO	R3081	
DP_XA_HPD	ARKANOID:HPD	R3082	ARKANOID_P7
SMC_DEBUGPRT_TX_L	ARKANOID:MOJO	R3083	

F3000 CRITICAL 6AMP-32V-0.0095OHM =PP20V_USBC_XA_VBUS — PP20V_USBC_XA_VBUS_F (0603)

F3010 CRITICAL 6AMP-32V-0.0095OHM =PP20V_USBC_XB_VBUS — PP20V_USBC_XB_VBUS_F (0603)

POWER ALIASES

=PP3V3_G3H_UPC_XA	PP3V3_G3H_UPC_XA	R3000	PP3V3_G3H
=PP3V3_G3H_UPC_XB	PP3V3_G3H_UPC_XB	R3001	PP3V3_G3H

MAKE_BASE=TRUE; 5% 1/20W MF 0201

=PP20V_USBC_XA_VBUS	PP20V_USBC_XA_VBUS
=PP20V_USBC_XB_VBUS	PP20V_USBC_XB_VBUS
=UPC_XA_I2C_STRAP	PP3V3_UPC_XA_LDO
=PP3V3R1V8_UPC_XA	
=UPC_XB_I2C_STRAP	PP3V3_UPC_XB_LDO
=PP3V3_TBT_X_FLASH	
=PP3V3R1V8_UPC_XB	
=PP3V3_TBT_X_S0	PP3V3_TBT_X_S0
=PPHV_INT_G3H	

MISC ALIASES

=UPC_X_SPI_CLK	UPC_X_SPI_CLK
=UPC_X_SPI_CS_L	UPC_X_SPI_CS_L
=UPC_X_SPI_MOSI	UPC_X_SPI_MOSI
=UPC_X_SPI_MISO	UPC_X_SPI_MISO
USBC_X_POC_RESET	TBT_POC_RESET
TBT_X_RTD3_CIO_PWR_EN	TBT_X_CIO_PWR_EN
TBT_X_RTD3_USB_PWR_EN	TBT_X_USB_PWR_EN
TBT_X_PLUG_EVENT_L	TBT_X_CIO_PLUG_EVENT_L
=TBT_X_BATLOW_L	PM_BATLOW_L
=USBC_TMS_X_SWD_CLK_X	JTAG_TBT_X_TMS
=USBC_TMS_T_SWD_DATA_X	PU_USBC_TMS_T_SWD_DATA_X
JTAG_TBT_TDO	JTAG_ISP_TDO
=USBC_XA_RESET_L	TP_USBC_XA_RESET_L
UPC_XA_SPI_CLK	
UPC_XA_SPI_CS_L	
UPC_XA_SPI_MISO	
UPC_XA_SPI_MOSI	
UPC_XA_RESET	
UPC_XB_RESET	

MAKE_BASE=TRUE

XW3001 SM — PLACE_NEAR=U2800.A1:5MM; NO_XNET_CONNECTION=1 — P0V9_TBT_X_SVR_AGND (MIN_LINE_WIDTH=0.2000; MIN_NECK_WIDTH=0.2000; VOLTAGE=0V)

I2C_TBT_X_SDA			=I2C_UPC_XA_SDA1
I2C_TBT_X_SCL		UPC XA - U3100	=I2C_UPC_XA_SCL1
I2C_TBT_XA_INT_L		(WRITE: 0X70 READ: 0X71)	=I2C_UPC_XA_INT1_L
I2C_TBT_XB_INT_L			=I2C_UPC_XB_SDA1
		UPC XB - U3200	=I2C_UPC_XB_SCL1
		(WRITE: 0X7E READ: 0X7F)	=I2C_UPC_XB_INT1_L

TBT - MASTER
ALPINE RIDGE - U2800

TBT_X_SPI_CLK	R3098	100	TBT_X_SPI_CLK_DBG
TBT_X_SPI_CS_L	R3090	15	UPC_XB_SPI_CLK
TBT_X_SPI_MOSI	R3091	15	UPC_XB_SPI_CS_L
TBT_X_SPI_MISO	R3092	15	UPC_XB_SPI_MOSI
	R3093	15	UPC_XB_SPI_MISO
	R3094	15	=UPC_X_SPI_CLK
	R3095	15	=UPC_X_SPI_CS_L
	R3096	15	=UPC_X_SPI_MOSI
	R3097	15	=UPC_X_SPI_MISO

5% 1/20W MF 201

TBT_X_XTAL25M_OUT — C3002 20PF (5% C0G 25V 0201) — TBT_X_XTAL25M_IN

NOSTUFF R3006 1M 5% 1/20W MF 201

CRITICAL Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM

USB3_EXTA_R2D_C_P	C3020	0.1UF	USB3_EXTA_R2D_P — TP3091
USB3_EXTA_R2D_C_N	C3021	0.1UF	USB3_EXTA_R2D_N — TP3092
USB3_EXTA_D2R_P			TP3093
USB3_EXTA_D2R_N			TP3094

0201 X5R-CERM 10% 16V; SM-TPP3

USBC_XA_USB_TOP_P	USBC_XA_USB_DBG_TOP_P
USBC_XA_USB_TOP_N	USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_BOT_P	USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_BOT_N	USBC_XA_USB_DBG_BOT_N

MAKE_BASE=TRUE

CRITICAL L3000 90-OHM-0.1A EXCX4CE (2X1.6X1.6)

=USB_UPC_XA_P	USB_UPC_XA_F_P	=USB_UPC_XA_F_P
=USB_UPC_XA_N	USB_UPC_XA_F_N	=USB_UPC_XA_F_N

MAKE_BASE=TRUE; PLACE_NEAR=U3100.L5:5MM; PLACE_NEAR=U3100.K5:5MM

TP_UPC_XB_SWD_CLK — TSP_UPC_XB_SWD_CLK (MAKE_BASE=TRUE) — TP3090

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DP / USB SOURCE ALIASES

DP_DDI1_ML_C_P<3..0>		DP_X_SNK1_ML_C_P<3..0>
DP_DDI1_ML_C_N<3..0>		DP_X_SNK1_ML_C_N<3..0>
DP_DDI1_AUXCH_C_P		DP_X_SNK1_AUXCH_C_P
DP_DDI1_AUXCH_C_N		DP_X_SNK1_AUXCH_C_N
DP_DDPB_HPD		DP_X_SNK1_HPD
DP_DDI2_ML_C_P<3..0>		DP_X_SNK0_ML_C_P<3..0>
DP_DDI2_ML_C_N<3..0>		DP_X_SNK0_ML_C_N<3..0>
DP_DDI2_AUXCH_C_P		DP_X_SNK0_AUXCH_C_P
DP_DDI2_AUXCH_C_N		DP_X_SNK0_AUXCH_C_N
DP_DDPC_HPD		DP_X_SNK0_HPD

MAKE_BASE=TRUE

USB_EXTB_P		USB_UPC_PCH_XA_P	=USB_UPC_XA_P
USB_EXTB_N		USB_UPC_PCH_XA_N	=USB_UPC_XA_N
USB_UPC_XA_P	R3012	0	
USB_UPC_XA_N	R3013	0	
UPC_XA_FAULT_L	R3008	0	USB_EXTA_OC_L
NC_USB2_08P		USB_UPC_PCH_XB_P	=USB_UPC_XB_P
NC_USB2_08N		USB_UPC_PCH_XB_N	=USB_UPC_XB_N
USB_UPC_XB_P	R3014	0	
USB_UPC_XB_N	R3015	0	
UPC_XB_FAULT_L	R3018	0	USB_EXTB_OC_L

5% 1/20W MF 0201

PP3V3_TBT_X_LC

R3071	100K	TBT_X_HDMI_DDC_CLK	
R3035	100K	JTAG_TBT_TCK	R3033 0 — JTAG_ISP_TCK
R3036	100K	JTAG_TBT_TDI	R3034 0 — JTAG_ISP_TDI
R3073	100K	UPC_XA_DBG3	
R3074	100K	UPC_XA_DBG4	
R3072	100K	TBT_X_HDMI_DDC_DATA	
R3066	100K	DP_X_SNK0_DDC_DATA	=DP_X_SNK0_DDC_DATA
R3067	100K	DP_X_SNK0_DDC_CLK	=DP_X_SNK0_DDC_CLK
R3069	100K	DP_X_SNK1_DDC_CLK	=DP_X_SNK1_DDC_CLK
R3070	100K	DP_X_SNK1_DDC_DATA	=DP_X_SNK1_DDC_DATA
R3040	100K	PD_UPC_XA_GPIO5	UPC_XA_HPD_RX
R3041	100K	PD_UPC_XB_GPIO5	UPC_XB_HPD_RX
R3042	100K	PD_UPC_XA_GPIO6	UPC_XA_5V_EN
R3043	100K	PD_UPC_XB_GPIO6	UPC_XB_5V_EN
R3049	100K	PD_TBT_X_TMU_CLK_OUT	=TBT_X_TMU_CLK_OUT
R3050	100K	PD_TBT_X_GPIO_8	=TBT_X_GPIO_8
R3020	1M	DP_X_SRC_HPD	

5% 1/20W MF 201; MAKE_BASE=TRUE

XPD JTAG ISOLATION

PD WHEN NOT USED

LOCAL BULK CAP

=PP5V_USBC — CRITICAL C3000 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

UPC_XA_DBG1		SMC_TCK
UPC_XA_DBG2		SMC_TMS
UPC_XB_DBG1		SSD_JTAG_TCK
UPC_XB_DBG2		SSD_JTAG_TMS
UPC_XB_DBG3		SMC_DEBUGPRT_TX_L
UPC_XB_DBG4		SMC_DEBUGPRT_RX_L

MAKE_BASE=TRUE

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE: USB-C SUPPORT

Apple Inc.

DRAWING NUMBER: 051-02265 | SIZE: D
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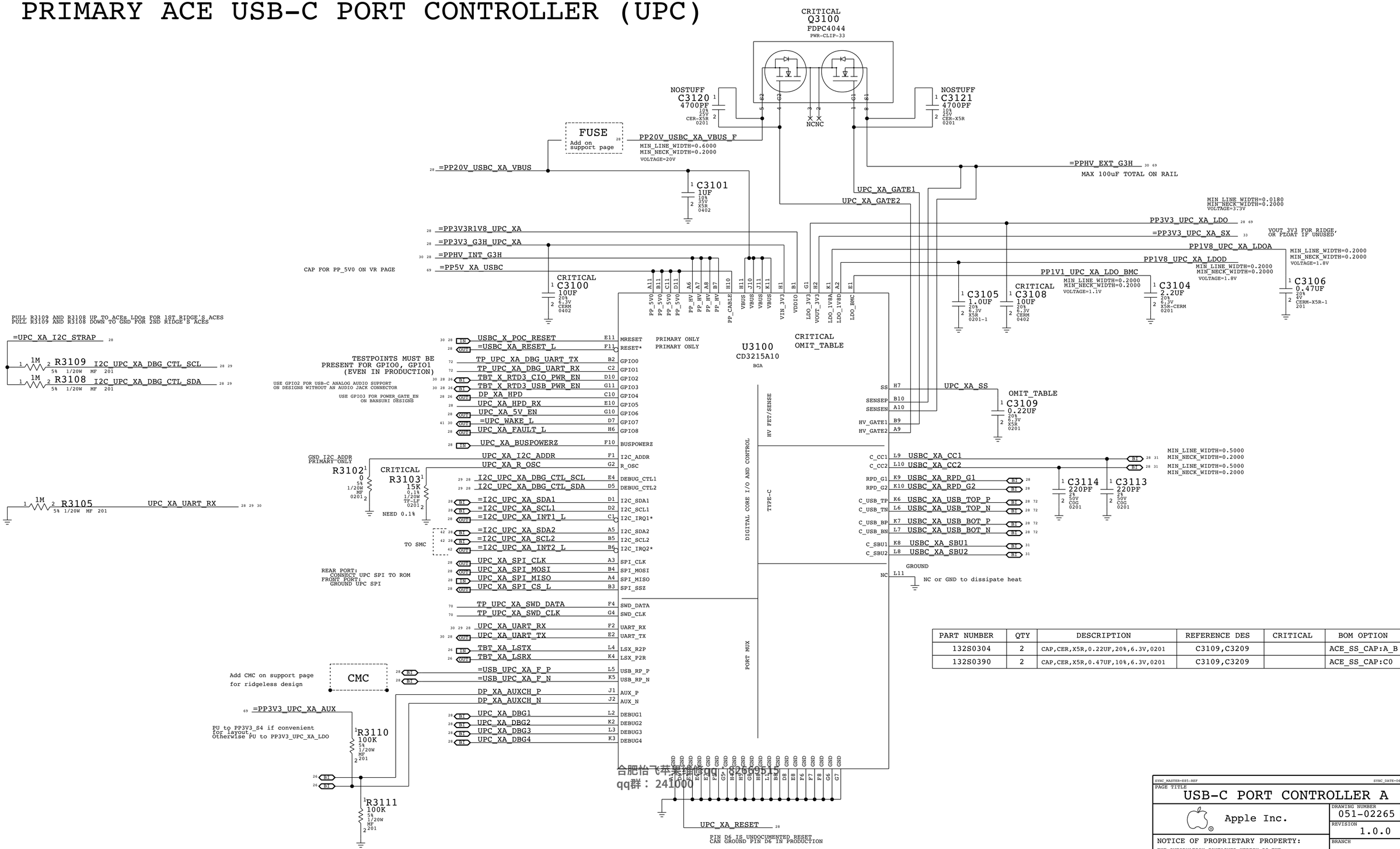
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0304	2	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C3109,C3209		ACE_SS_CAP:A_B
132S0390	2	CAP,CER,X5R,0.47UF,10%,6.3V,0201	C3109,C3209		ACE_SS_CAP:C0

合肥恰飞科技有限公司 QQ：2260051
qq群： 241000

SYNC_MASTER=E85-REF SYNC_DATE=06/17/2015

PAGE TITLE
USB-C PORT CONTROLLER A

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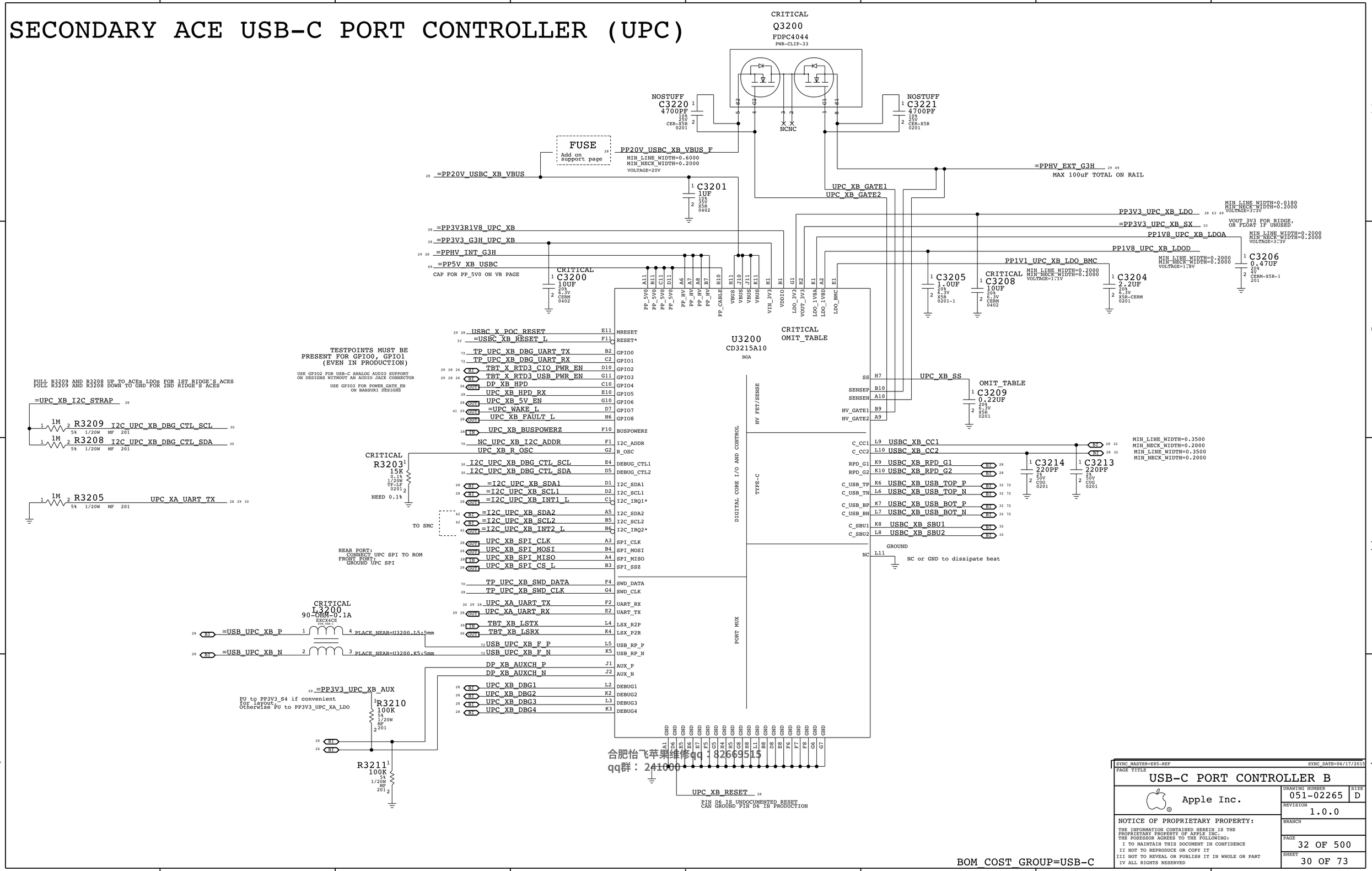
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



合肥怡飞苹果维修qq：82669515
qq群： 241000

SYNC_MASTER=E85-REF SYNC_DATE=06/17/2015

PAGE TITLE
USB-C PORT CONTROLLER B

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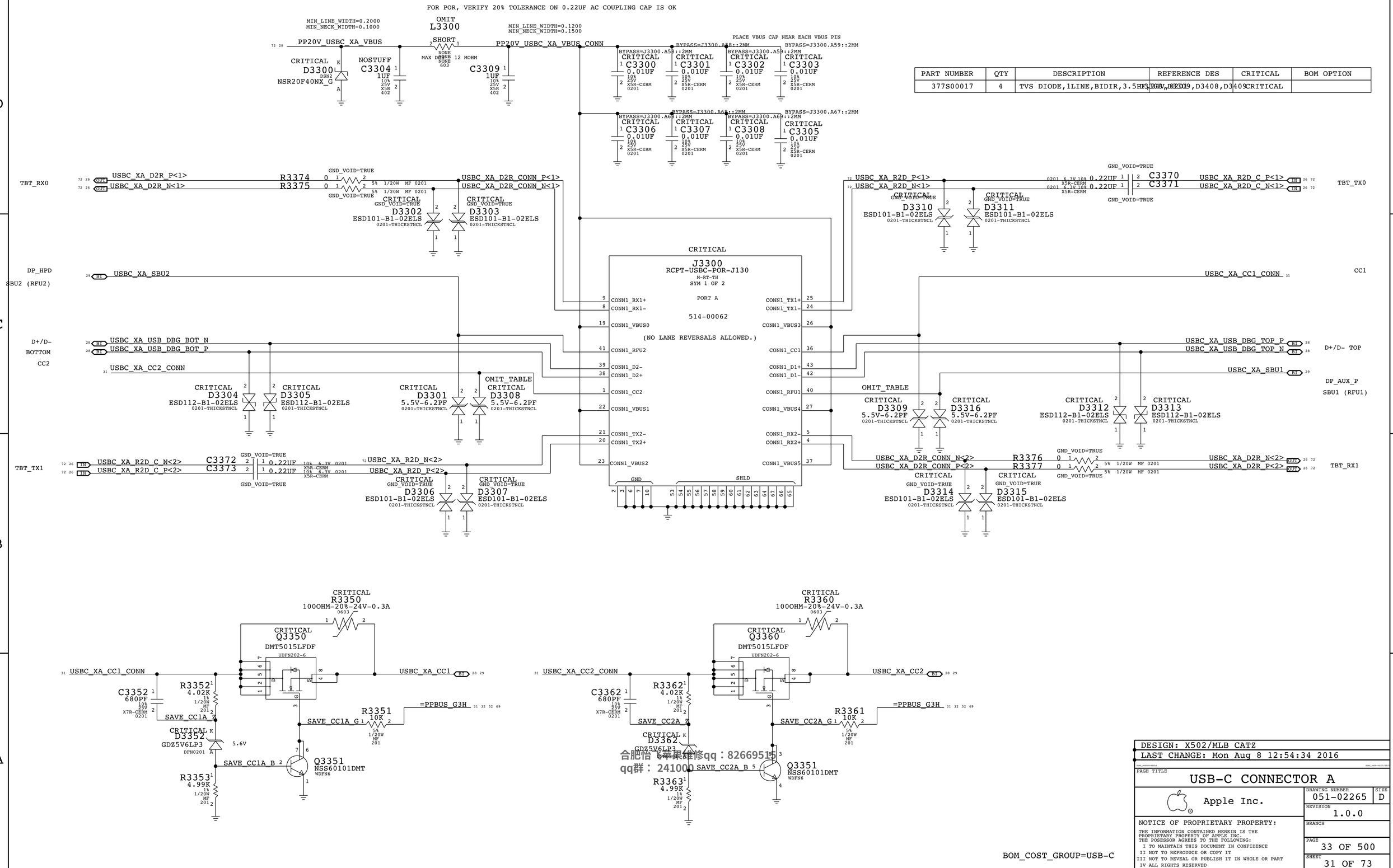
FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S00017	4	TVS DIODE,1LINE,BIDIR,3.5HF,3.0V,0.22PF	D3309,D3312,D3314,D3315,D3408,D3409	CRITICAL	



合肥恰 苹果维修qq：826695155
qq群： 241000

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
USB-C CONNECTOR A

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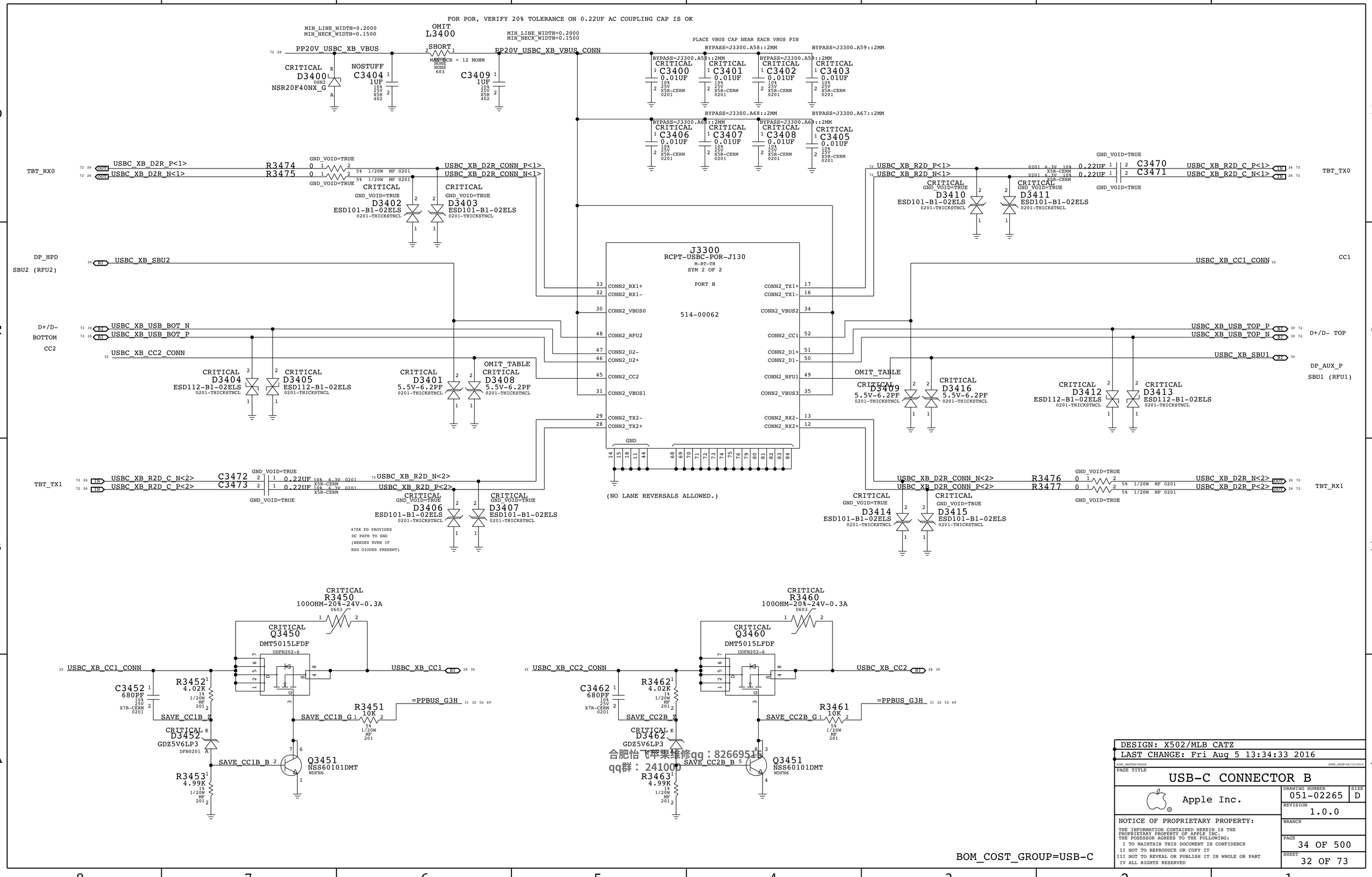

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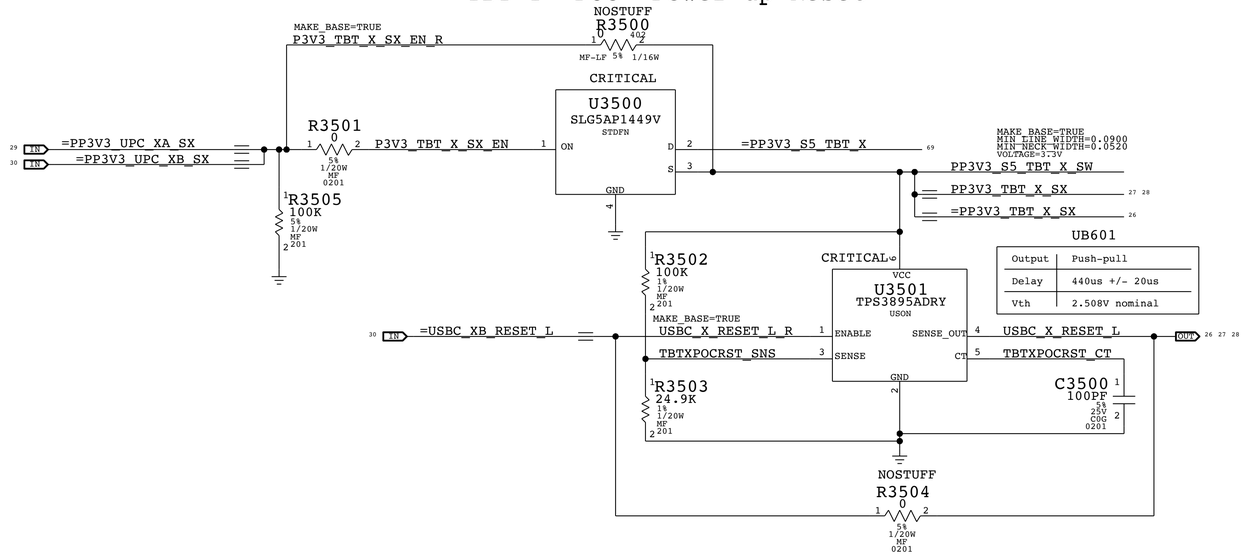
qq群： 241000

TBT T "POC" Power-up Reset



合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
USB-C SUPPORT 2

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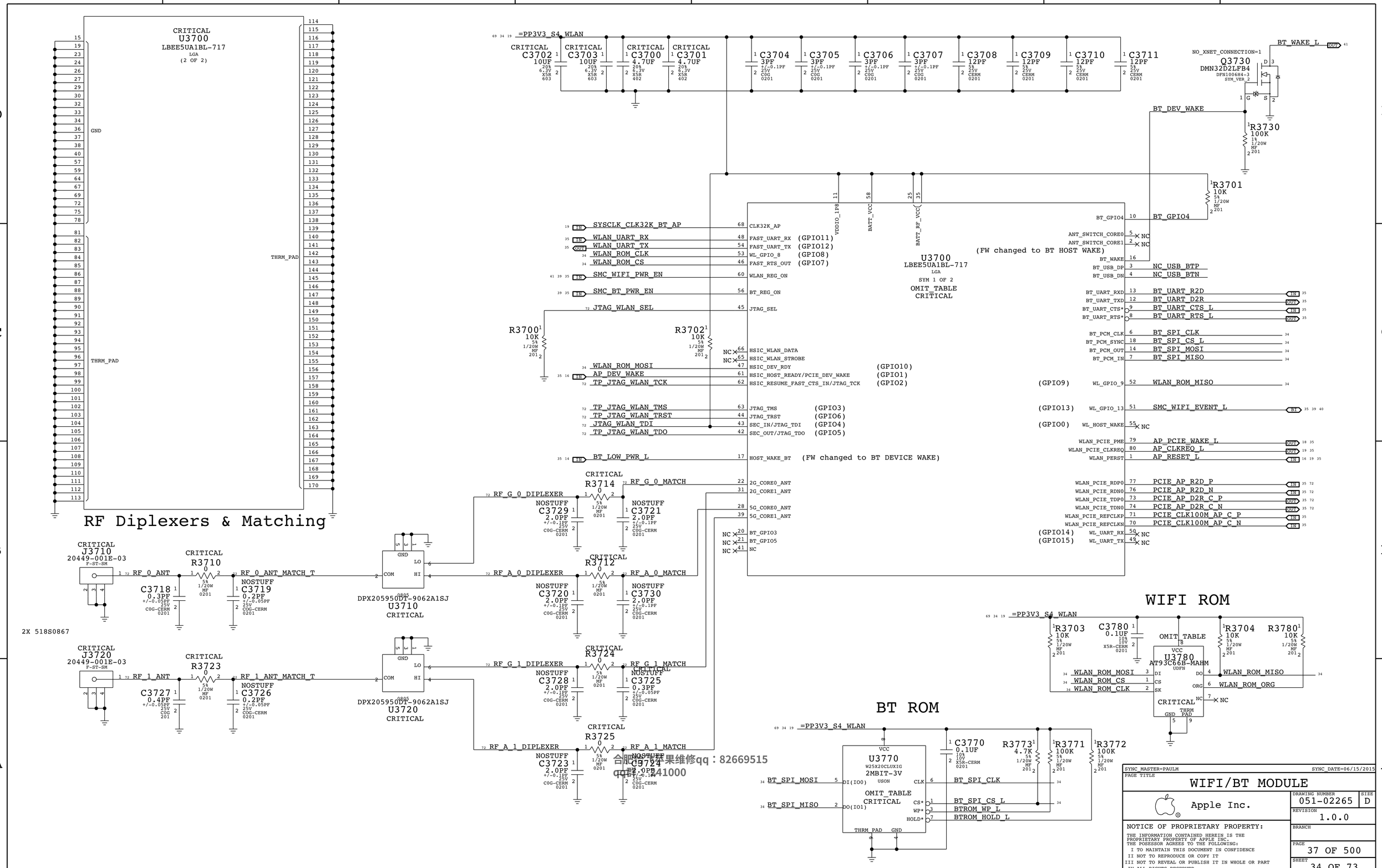

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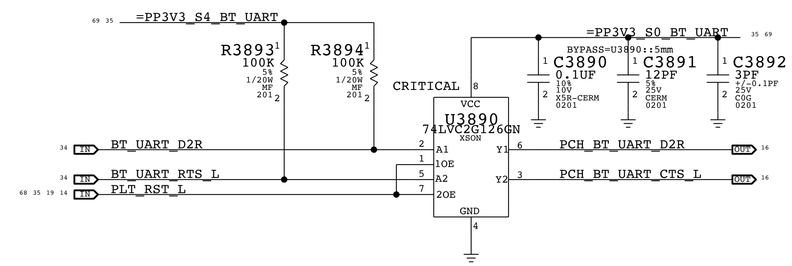
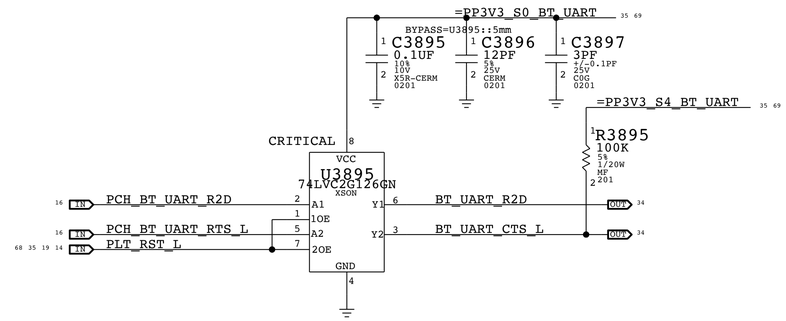
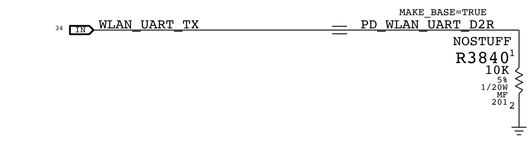
qq：2441000

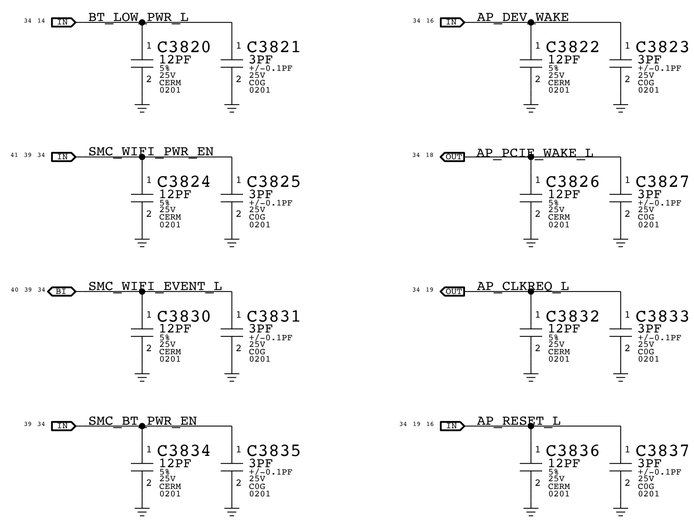
BT UART Isolation

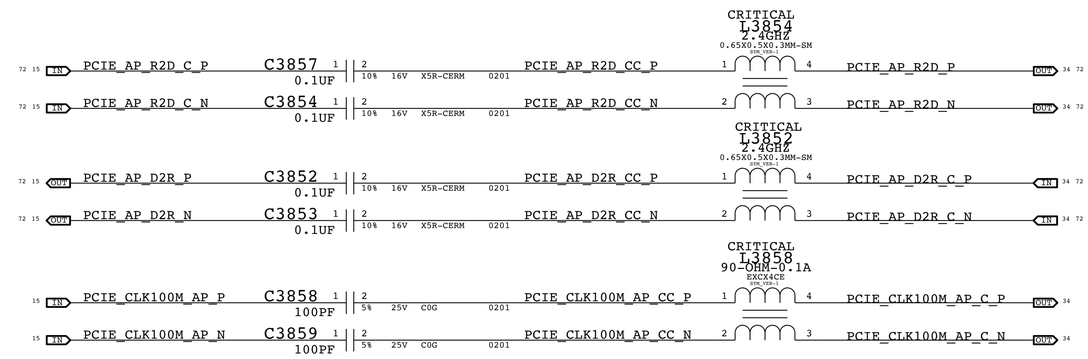




WIFI UART ISOLATION







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PAGE TITLE
WIFI/BT Module Support

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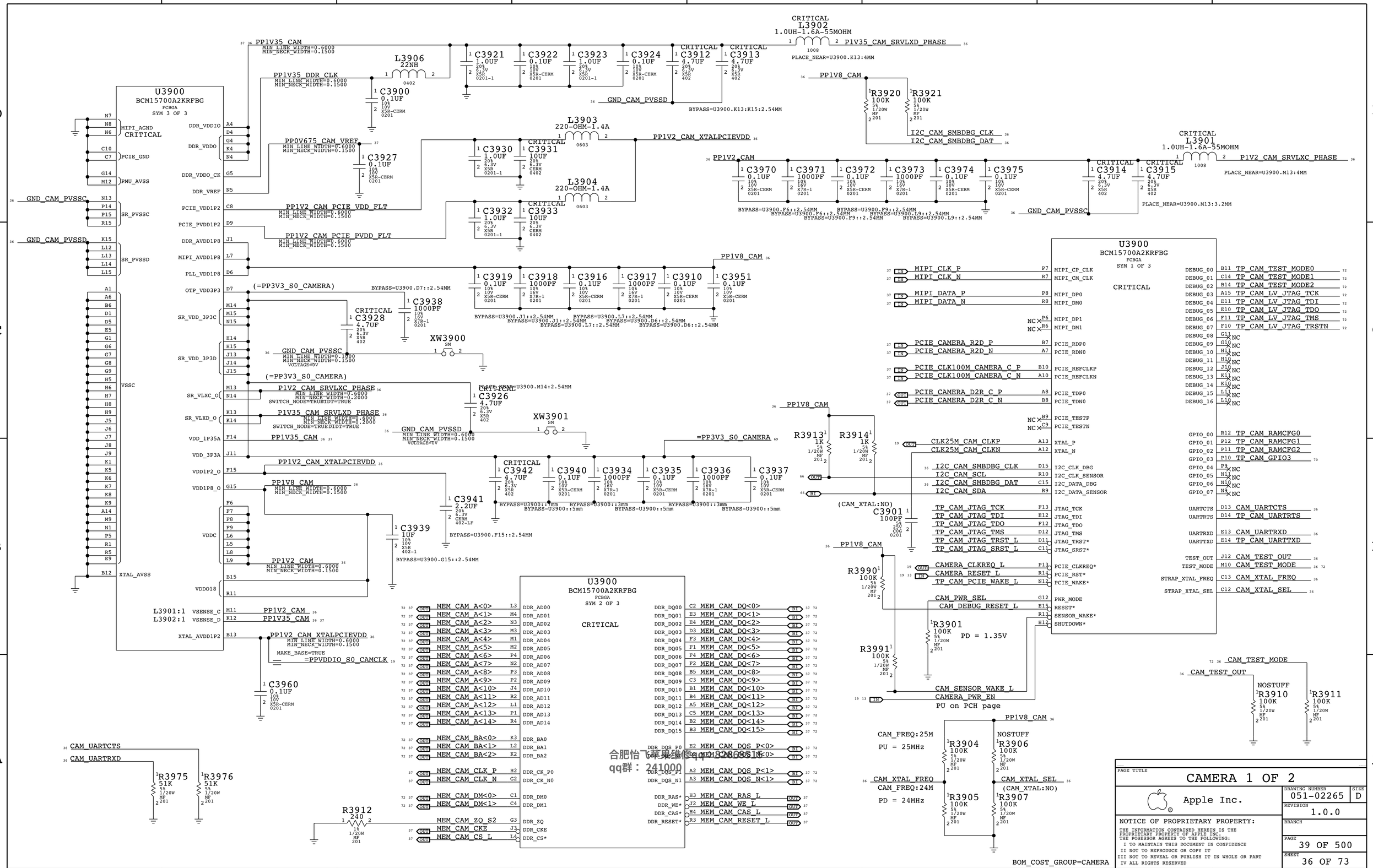
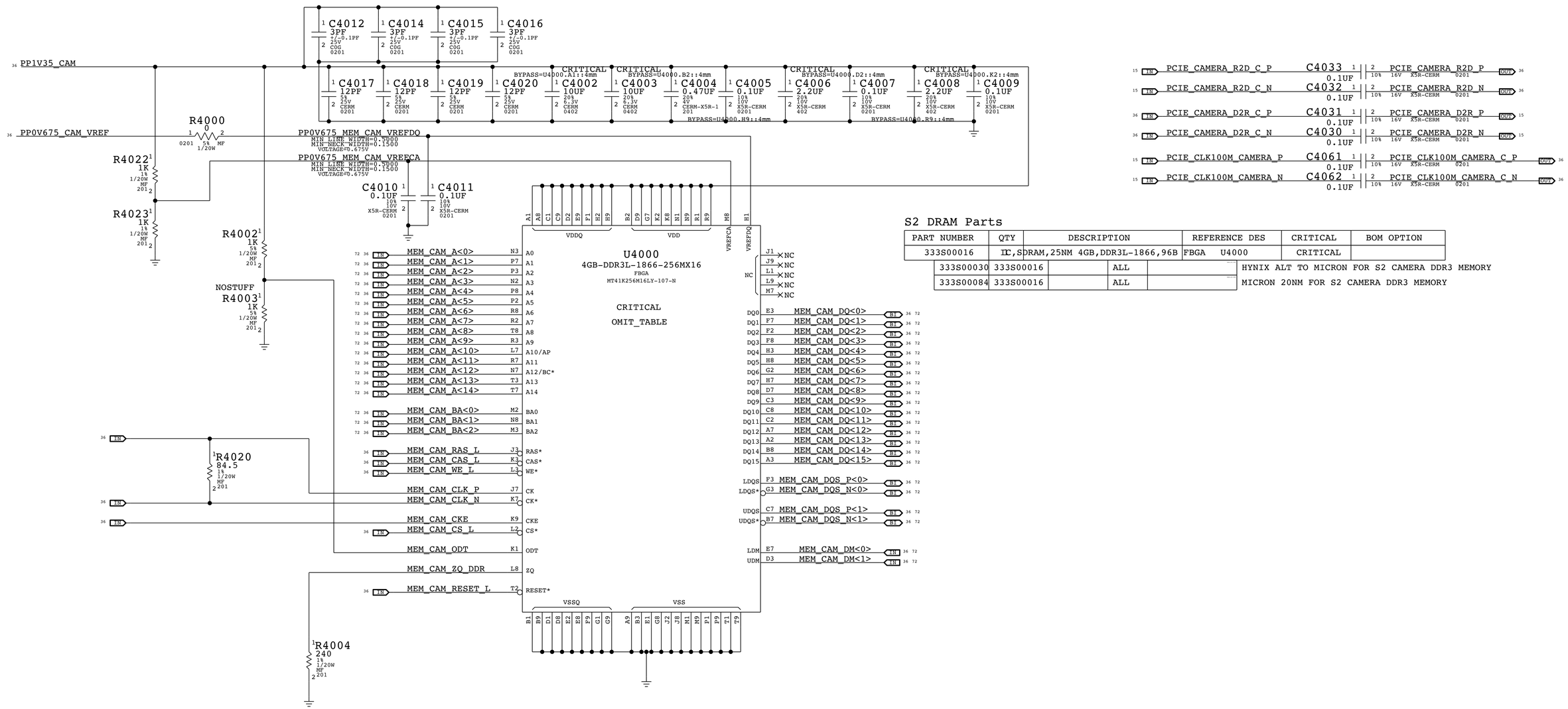


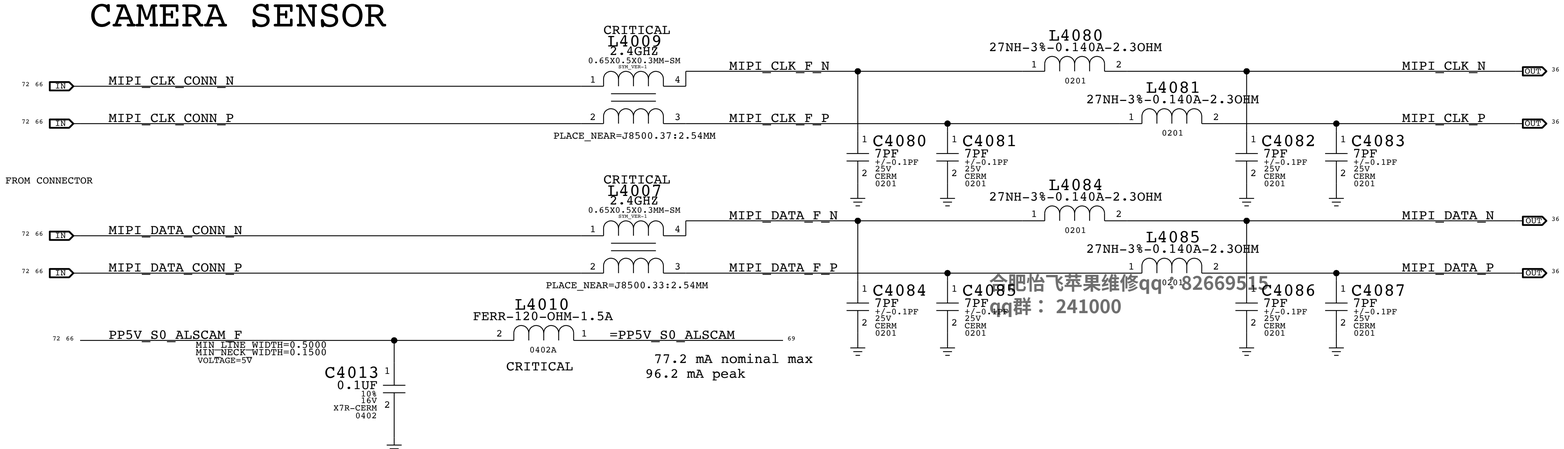
合肥怡飞苹果维修 QQ群：241000
qq群： 241000



S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00016	IC,SDRAM,25NM 4GB,DDR3L-1866,96B		FBGA U4000	CRITICAL	
333S00030	333S00016	ALL			HYNIX ALT TO MICRON FOR S2 CAMERA DDR3 MEMORY
333S00084	333S00016	ALL			MICRON 20NM FOR S2 CAMERA DDR3 MEMORY

CAMERA SENSOR



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qq群： 241000

BOM_COST_GROUP=CAMERA

PAGE TITLE: CAMERA 2 OF 2

Apple Inc.

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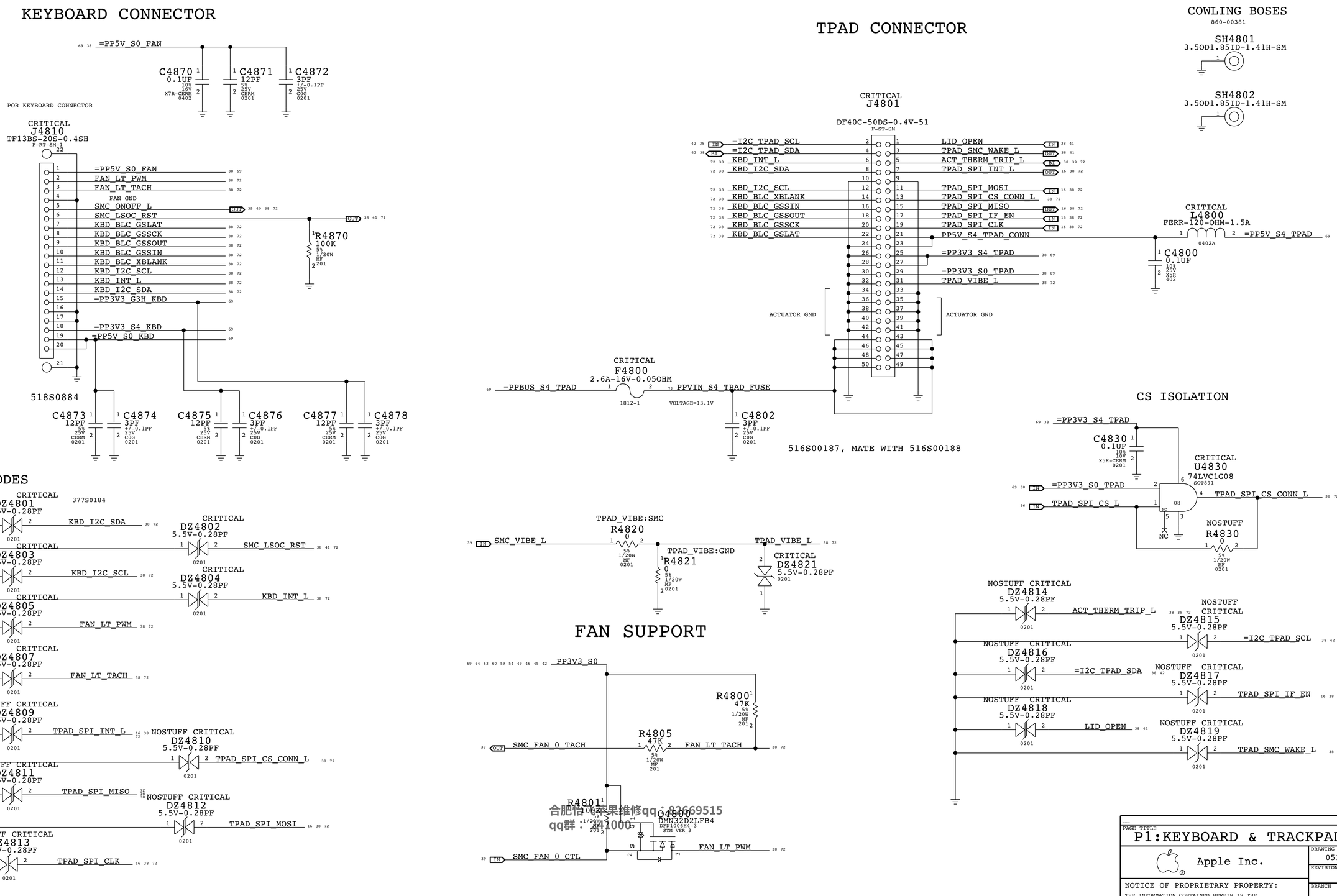

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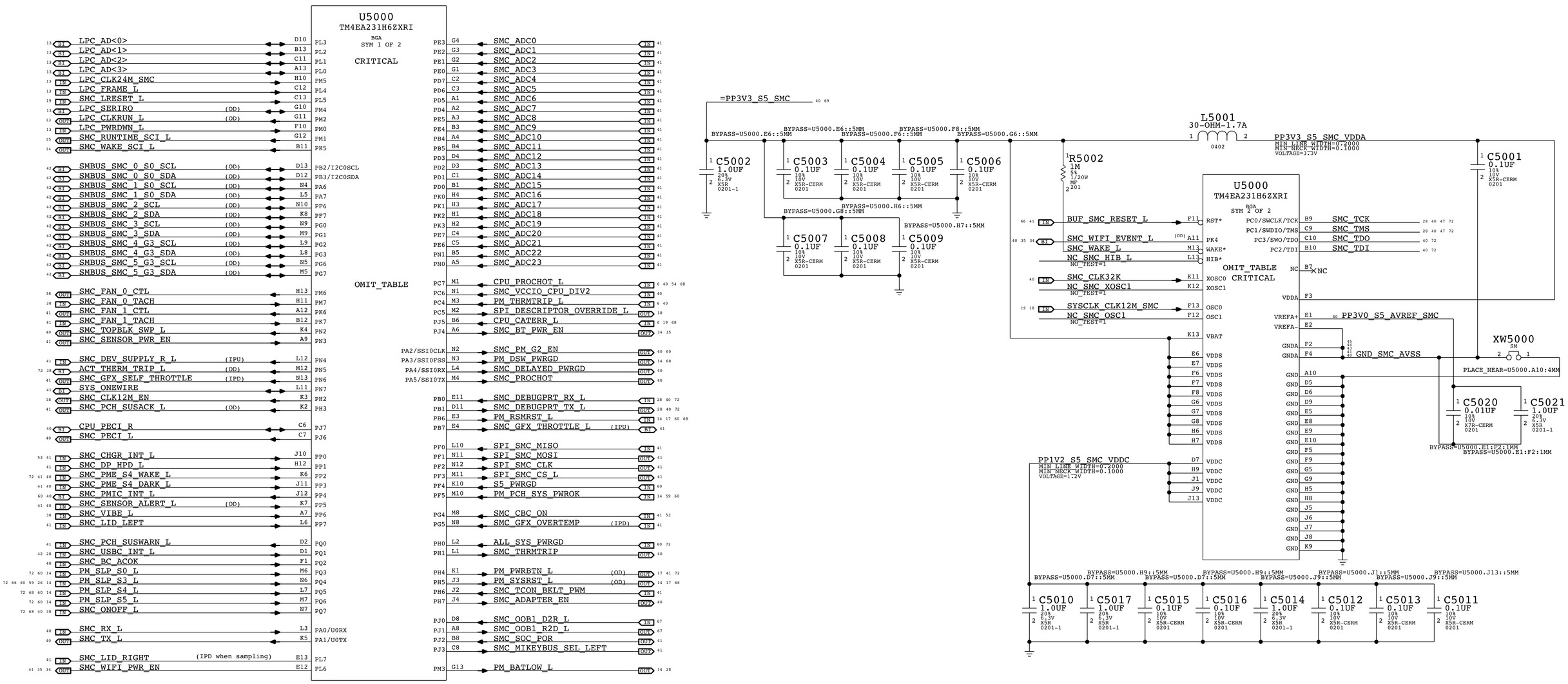
qq群：410000



NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

合肥怡飞苹果维修qq：82669515
qq群： 241000

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE
SMC

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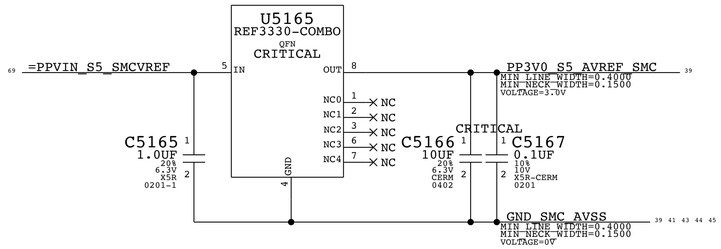
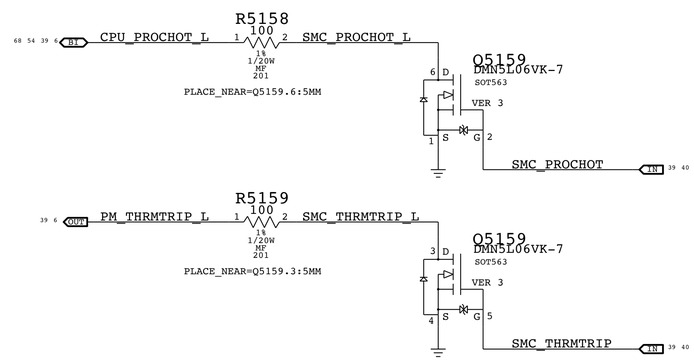
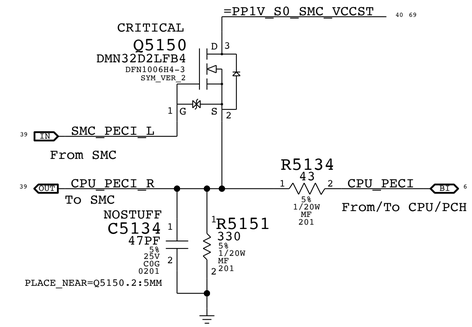
SMC AVREF Supply



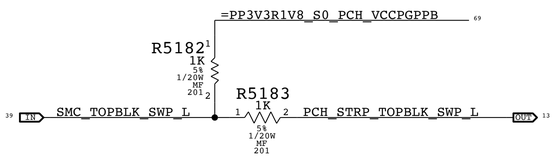
PROCHOT/THRMTRIP Support

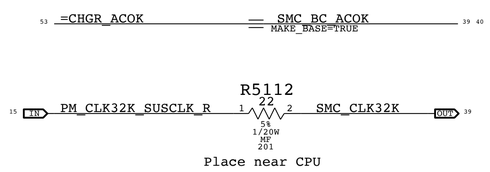


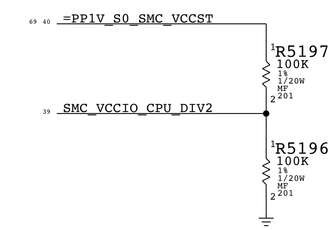
PECI Support

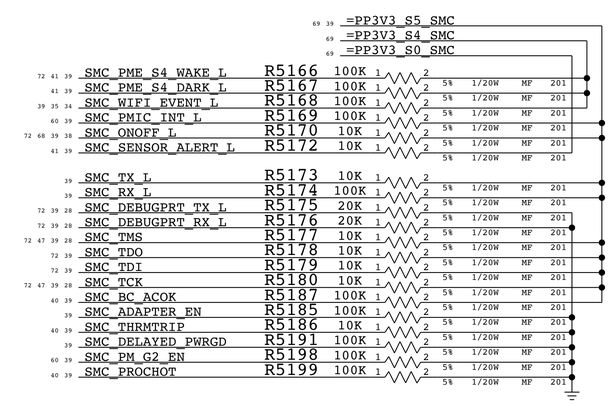


Top-Block Swap









合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=SMC

PAGE TITLE
SMC Shared Support

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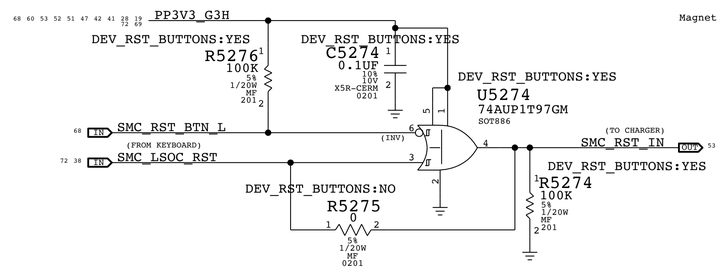
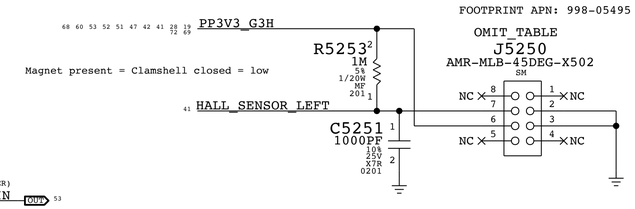
SMC ANALOG INPUTS

SMC_ADC0	MAKE_BASE=TRUE	SMC_DCIN_VSENSE	IN 43
SMC_ADC1	MAKE_BASE=TRUE	SMC_DCIN_ISENSE	IN 43
SMC_ADC2	MAKE_BASE=TRUE	SMC_PBUS_VSENSE	IN 43
SMC_ADC3	MAKE_BASE=TRUE	SMC_BMON_ISENSE	IN 43
SMC_ADC4	MAKE_BASE=TRUE	SMC_TPAD_ISENSE	IN 43
SMC_ADC5	MAKE_BASE=TRUE	SMC_CPU_HI_ISENSE	IN 43
SMC_ADC6	MAKE_BASE=TRUE	SMC_CPU_VSENSE	IN 45
SMC_ADC7	MAKE_BASE=TRUE	SMC_CPU_ISENSE	IN 45
SMC_ADC8	MAKE_BASE=TRUE	SMC_GT_VSENSE	IN 45
SMC_ADC9	MAKE_BASE=TRUE	SMC_GT_ISENSE	IN 45
SMC_ADC10	MAKE_BASE=TRUE	SMC_SA_ISENSE	IN 45
SMC_ADC11	MAKE_BASE=TRUE	SMC_1VS5G_ISENSE	IN 44
SMC_ADC12	MAKE_BASE=TRUE	SMC_SSD_ISENSE	IN 43
SMC_ADC13	MAKE_BASE=TRUE	SMC_3V3SSD_ISENSE	IN 44
SMC_ADC14	MAKE_BASE=TRUE	SMC_1V2S3_ISENSE	IN 44
SMC_ADC15	MAKE_BASE=TRUE	SMC_CPU_IMON_ISENSE	IN 45
SMC_ADC16	MAKE_BASE=TRUE	SMC_GT_IMON_ISENSE	IN 45
SMC_ADC17	MAKE_BASE=TRUE	SMC_3V3LCD_ISENSE	IN 44
SMC_ADC18	MAKE_BASE=TRUE	SMC_3V3WLS_ISENSE	IN 44
SMC_ADC19	MAKE_BASE=TRUE	SMC_LCDBKLT_ISENSE	IN 43
SMC_ADC20	MAKE_BASE=TRUE	SMC_SA_IMON_ISENSE	IN 45
SMC_ADC21	MAKE_BASE=TRUE	SMC_5VS4_ISENSE	IN 44
SMC_ADC22	MAKE_BASE=TRUE	SMC_3V3S5_ISENSE	IN 44
SMC_ADC23	MAKE_BASE=TRUE	SMC_TBT_ISENSE	IN 45

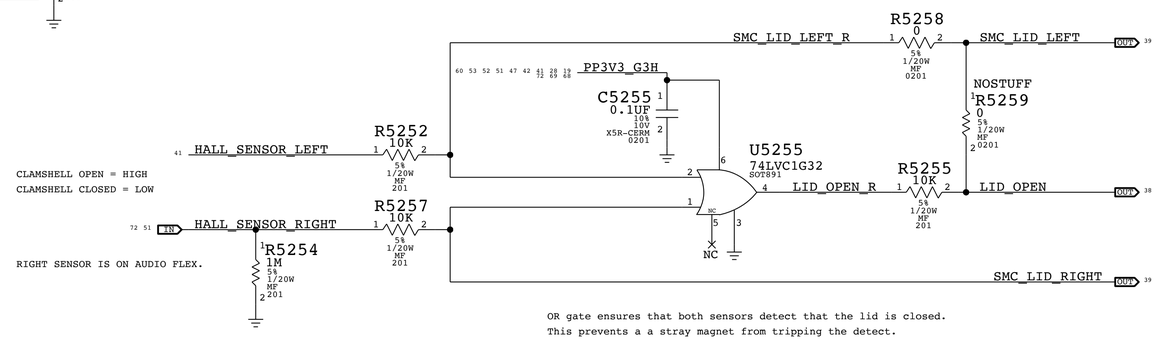
SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_THROTTLE_L
SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_OVERTEMP
SMC_FAN_1_CTL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_CTL
SMC_FAN_1_TACH	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_TACH
SMC_SOC_POR	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_SOC_POR
SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_SELF_THROTTLE
SPI_SMC_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CLK
SPI_SMC_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CS_L
SPI_SMC_MISO	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MISO
SPI_SMC_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MOSI
SMC_MIKEYBUS_SEL_LEFT	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_MIKEYBUS_SEL_LEFT
SYS_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1	NC_SYS_ONEWIRE



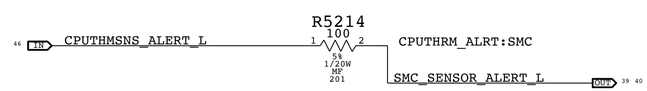
AMR SENSOR PADS

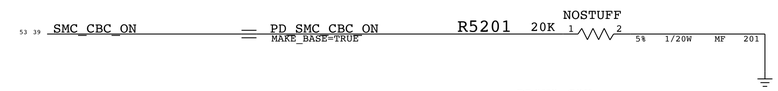


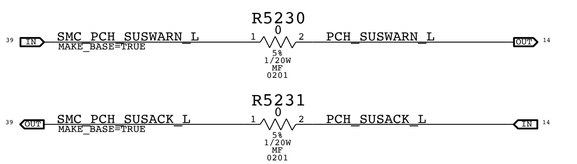
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-05143	1	SUBASSY (T&R) PCBA,HES INTERPOSER 45,X502	J5250	CRITICAL	



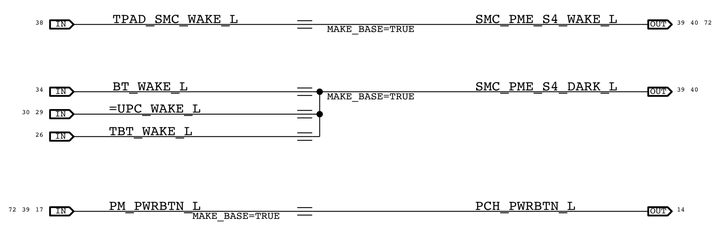
Thermal Alerts

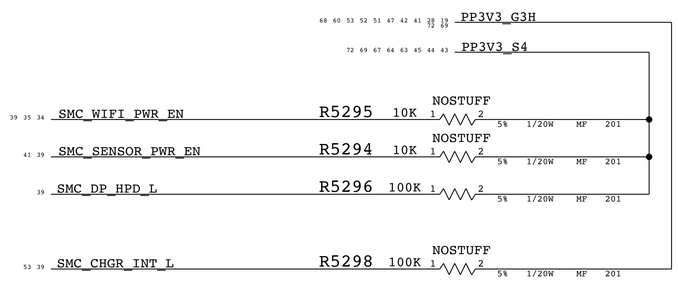


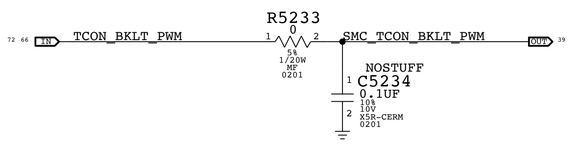


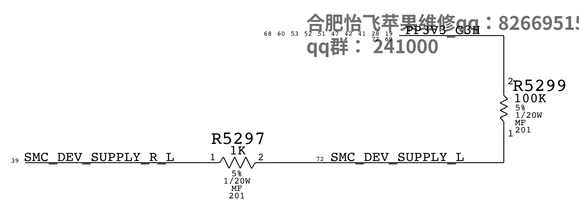


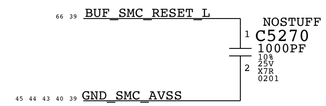
S4 SMC Wake Sources











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SYNC MASTER=PAULM

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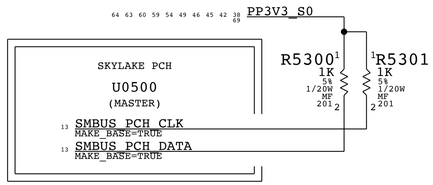
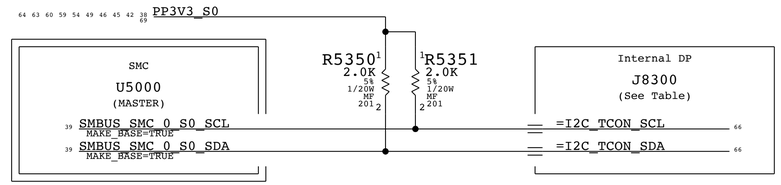
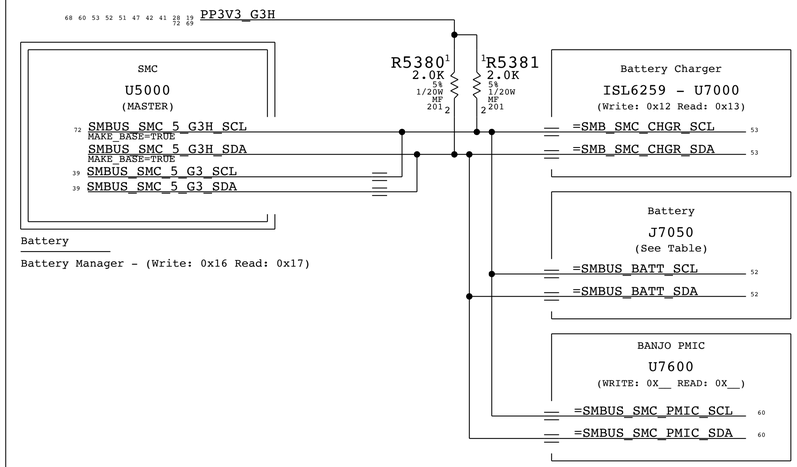
SKYLAKE PCH S0 "SMBUS 0" CONNECTIONS



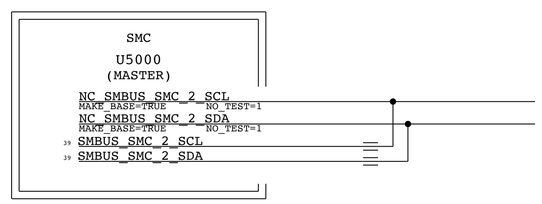
SMC SMBus "0" S0 Connections



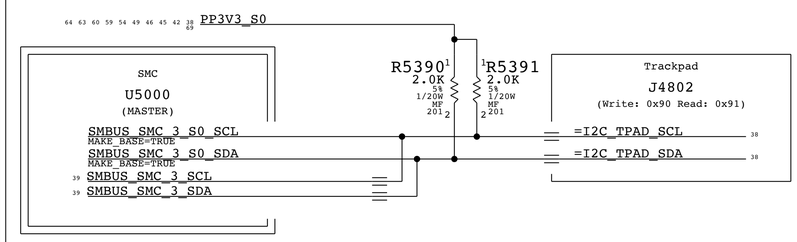
SMC SMBus "5" G3H Connections



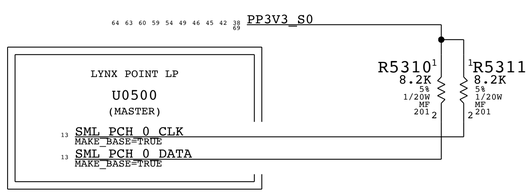
SMC SMBus "2" S3 Connections



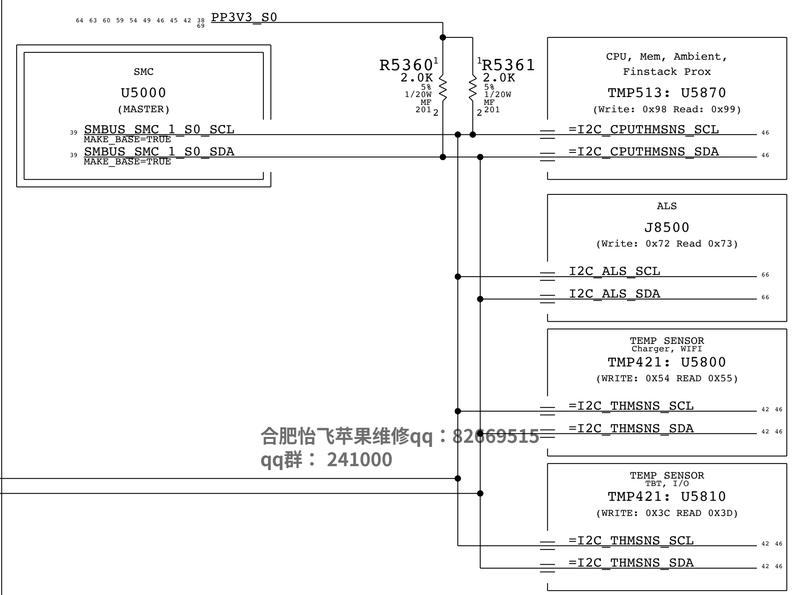
SMC SMBus "3" S0 Connections



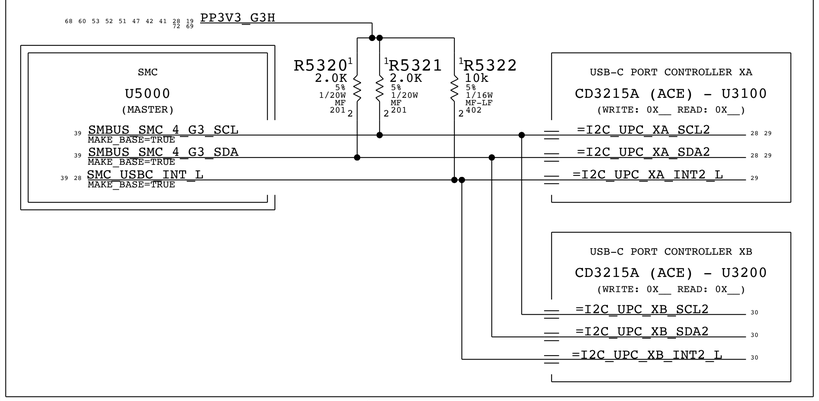
LYNX POINT LP S0 "SMLink 0" Connections



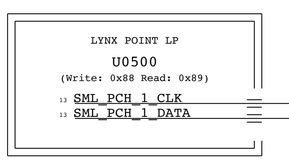
SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH.

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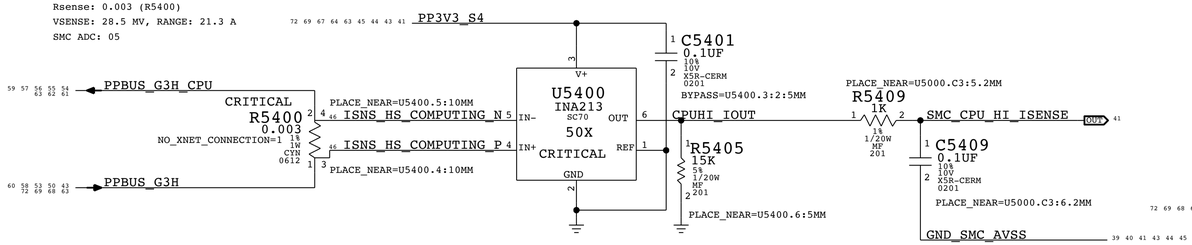
INA21X PARTS HAVE MINOR LEAKAGE PATH FROM INPUTS TO OUTPUT WHEN UNPOWERED.
PULL-DOWN RESISTERS ON INA OUTPUTS BLEED OFF THE LEAKAGE CURRENT TO PREVENT
SIGNAL PUMP-UP.

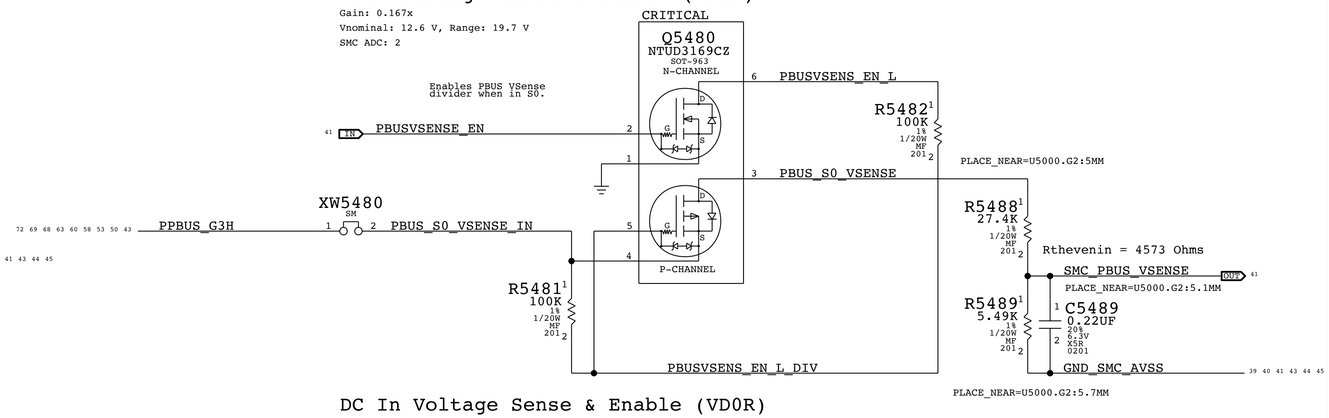
CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A
Rsense: 0.003 (R5400)
VSENSE: 28.5 MV, RANGE: 21.3 A
SMC ADC: 05



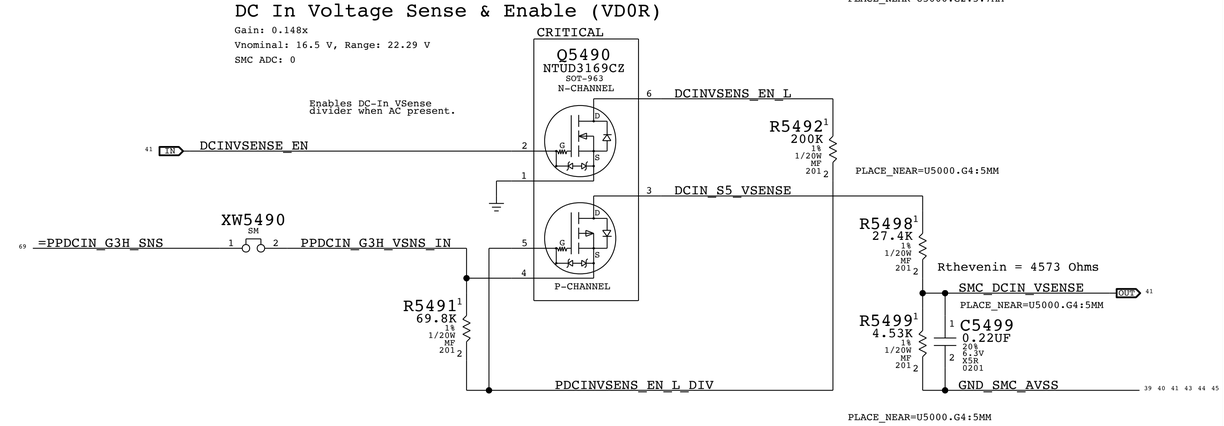
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 2



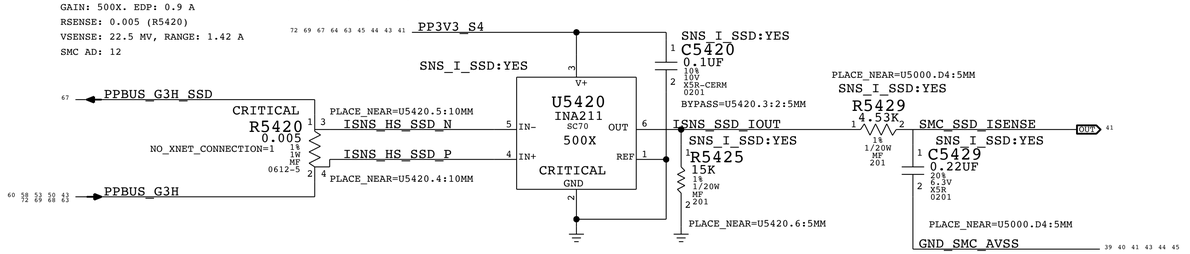
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 0



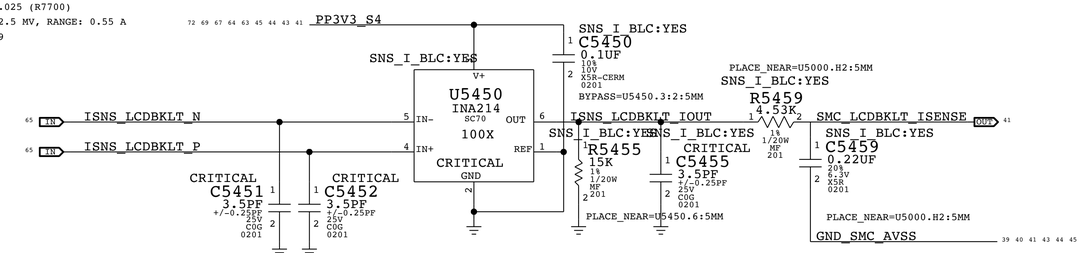
SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R5420)
VSENSE: 22.5 MV, RANGE: 1.42 A
SMC AD: 12



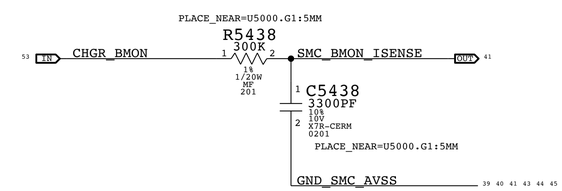
LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X. EDP: 0.9 A
Rsense: 0.025 (R7700)
VSENSE: 22.5 MV, RANGE: 0.55 A
SMC AD: 19



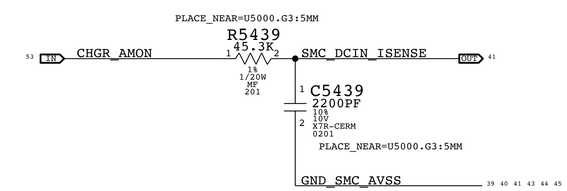
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
RSENSE: 0.005 (R7160)
SMC ADC: 03



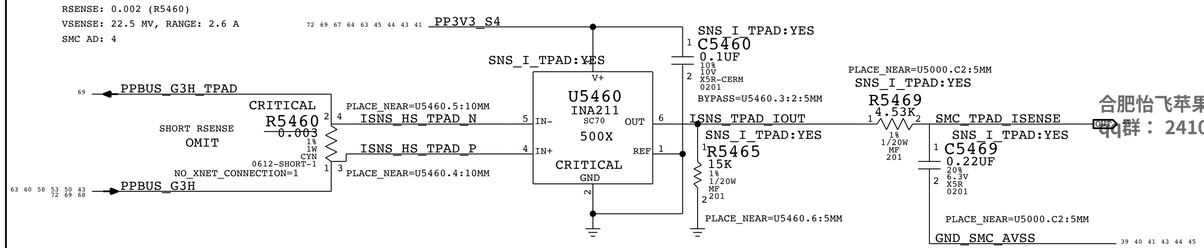
DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
RSENSE: 0.010 (R7120)
SMC ADC: 01



TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R5460)
VSENSE: 22.5 MV, RANGE: 2.6 A
SMC AD: 4



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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5429		SNS_I_SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

BOM_COST_GROUP=SENSORS

DESIGN: X502/MLB CATZ
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Power Sensors High Side

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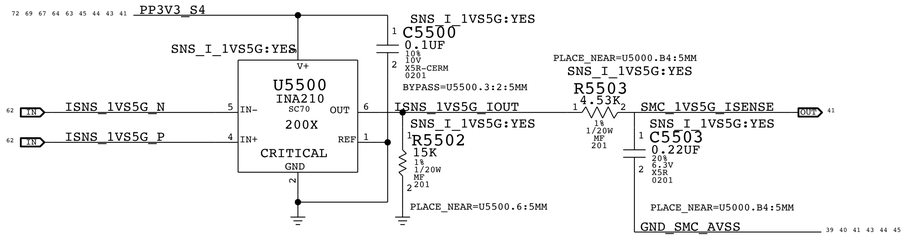
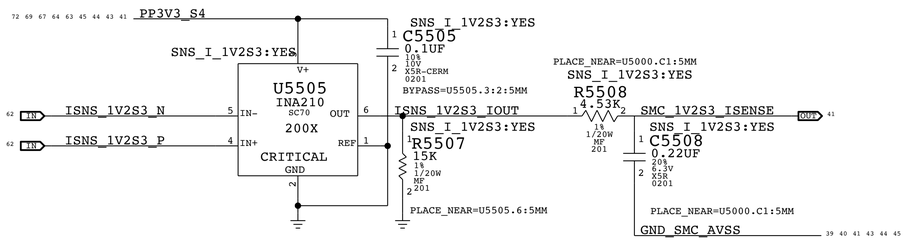
1V_S5G CURRENT SENSE (ISIC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7700)
VSENSE: 22.5 MV, RANGE: 3.0 A
SMC AD: 11



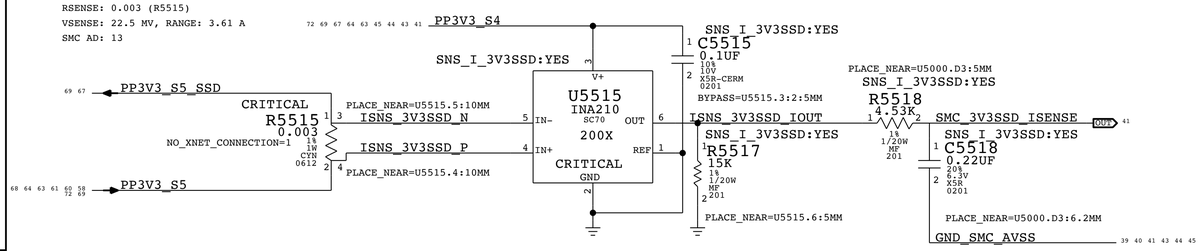
1V2_S3 CURRENT SENSE (IM0C)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 14



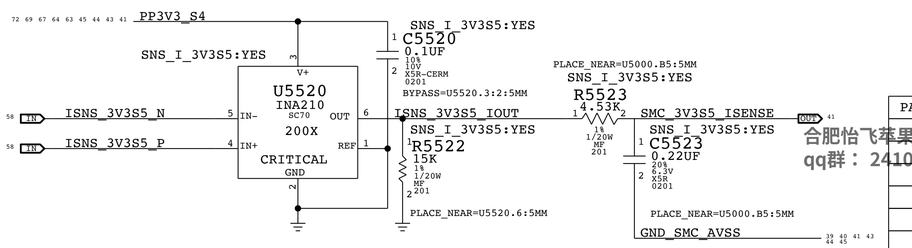
3V3_SSD CURRENT SENSE (IHCC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R5515)
VSENSE: 22.5 MV, RANGE: 3.61 A
SMC AD: 13



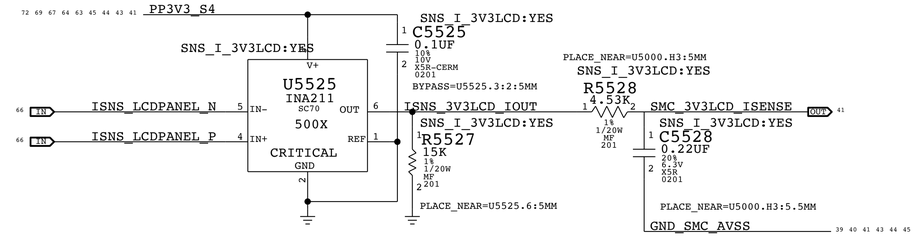
3V3_S5 CURRENT SENSE (IO3R) (HIGH-SIDE)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7710)
VSENSE: 22.5 MV ?, RANGE: 4 A
SMC AD: 22



3V3_S0 LCD CURRENT SENSE (ILDC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R5525)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

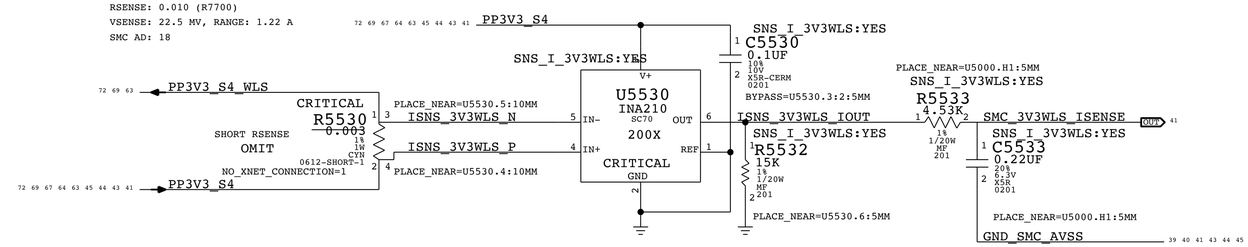


5V_S0 LCD CURRENT SENSE (I___)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R8520)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

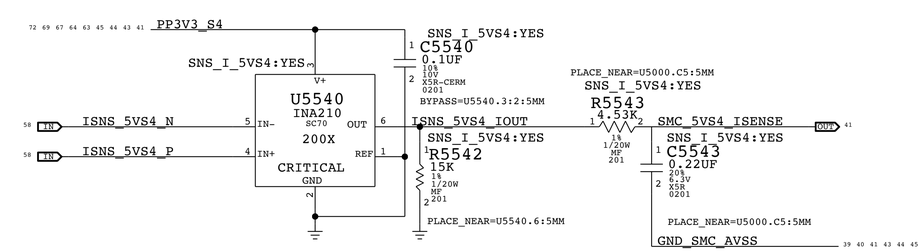
3V3_S4 WIRELESS CURRENT SENSE (IAPC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.010 (R7700)
VSENSE: 22.5 MV, RANGE: 1.22 A
SMC AD: 18



5V_S4 CURRENT SENSE (IO5R) (HIGH-SIDE)

GAIN: 200X. EDP: ?? A
RSENSE: 0.003 (R7900)
VSENSE: 22.5 MV ?, RANGE: 6.8 A
SMC AD: 21



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5508		SNS_I_1V2S3:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5518		SNS_I_3V3SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5523		SNS_I_3V3S5:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5528		SNS_I_3V3LCD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5533		SNS_I_3V3WLS:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5543		SNS_I_5VS4:NO

BOM_COST_GROUP=SENSORS

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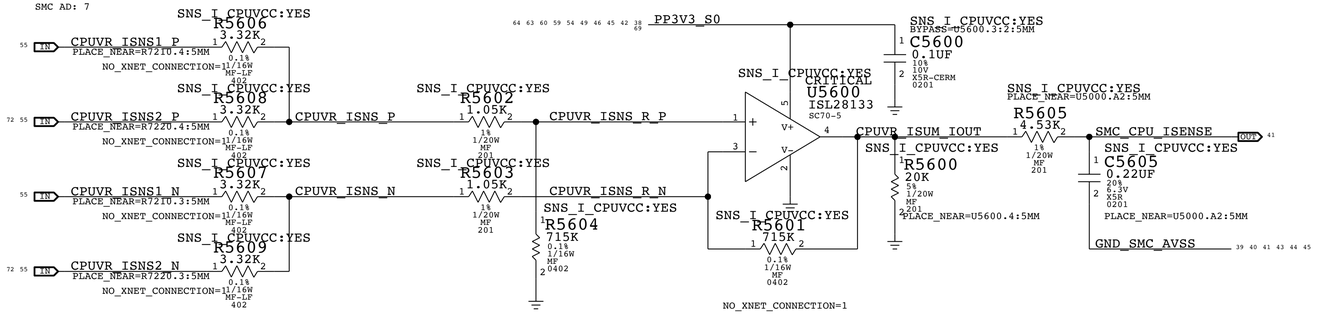
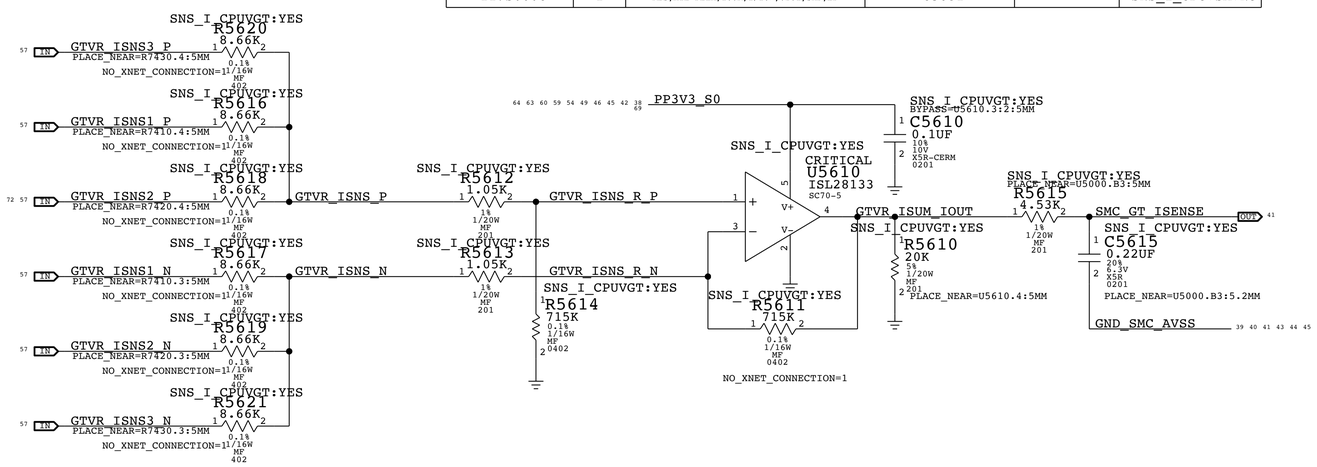
CPU VCC CURRENT SENSE (ICAC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 7



CPU GT CURRENT SENSE (ICGC)

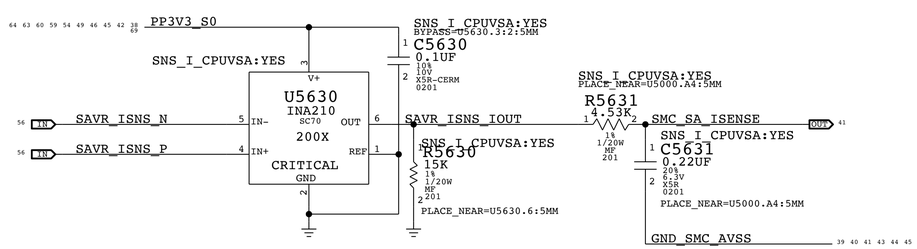
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 9



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO

CPU SA CURRENT SENSE (ICSC)

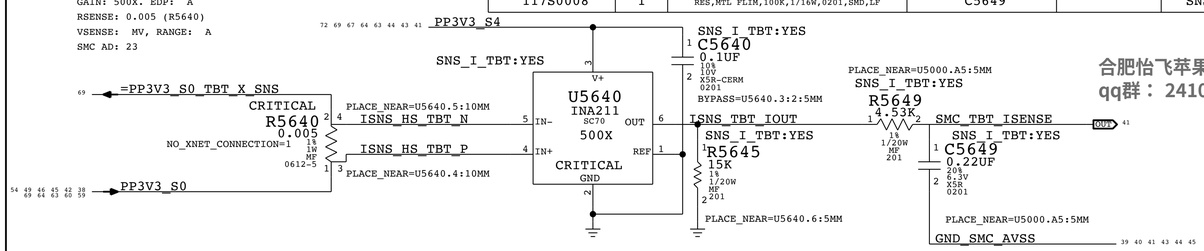
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 10



TBT CURRENT SENSE (IULC)

GAIN: 500X. EDP: A
RSENSE: 0.005 (R5640)
VSENSE: MV, RANGE: A
SMC AD: 23

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO



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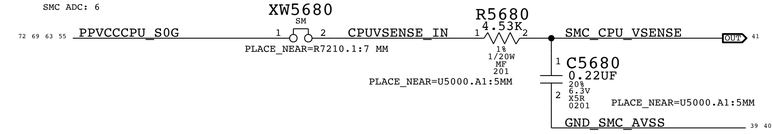
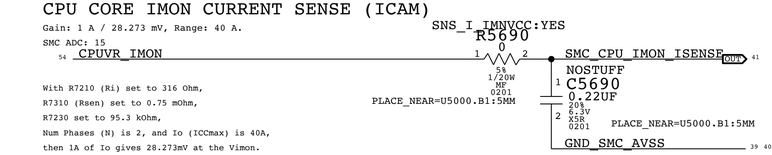
CPU CORE VOLTAGE SENSE (VCAC)

SMC ADC: 6



CPU CORE IMON CURRENT SENSE (ICAM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 15

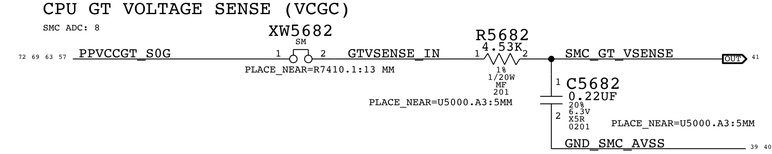


With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5690		SNS_I_IMNVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5692		SNS_I_IMNVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5691		SNS_I_IMNVSA:NO

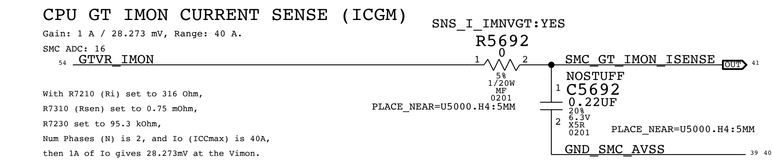
CPU GT VOLTAGE SENSE (VCGC)

SMC ADC: 8



CPU GT IMON CURRENT SENSE (ICGM)

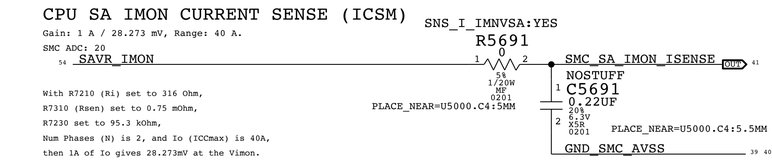
Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 16



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 20



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

BOM_COST_GROUP=SENSORS

DESIGN: X502/MLB CATZ
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PAGE TITLE
Power Sensors Extended

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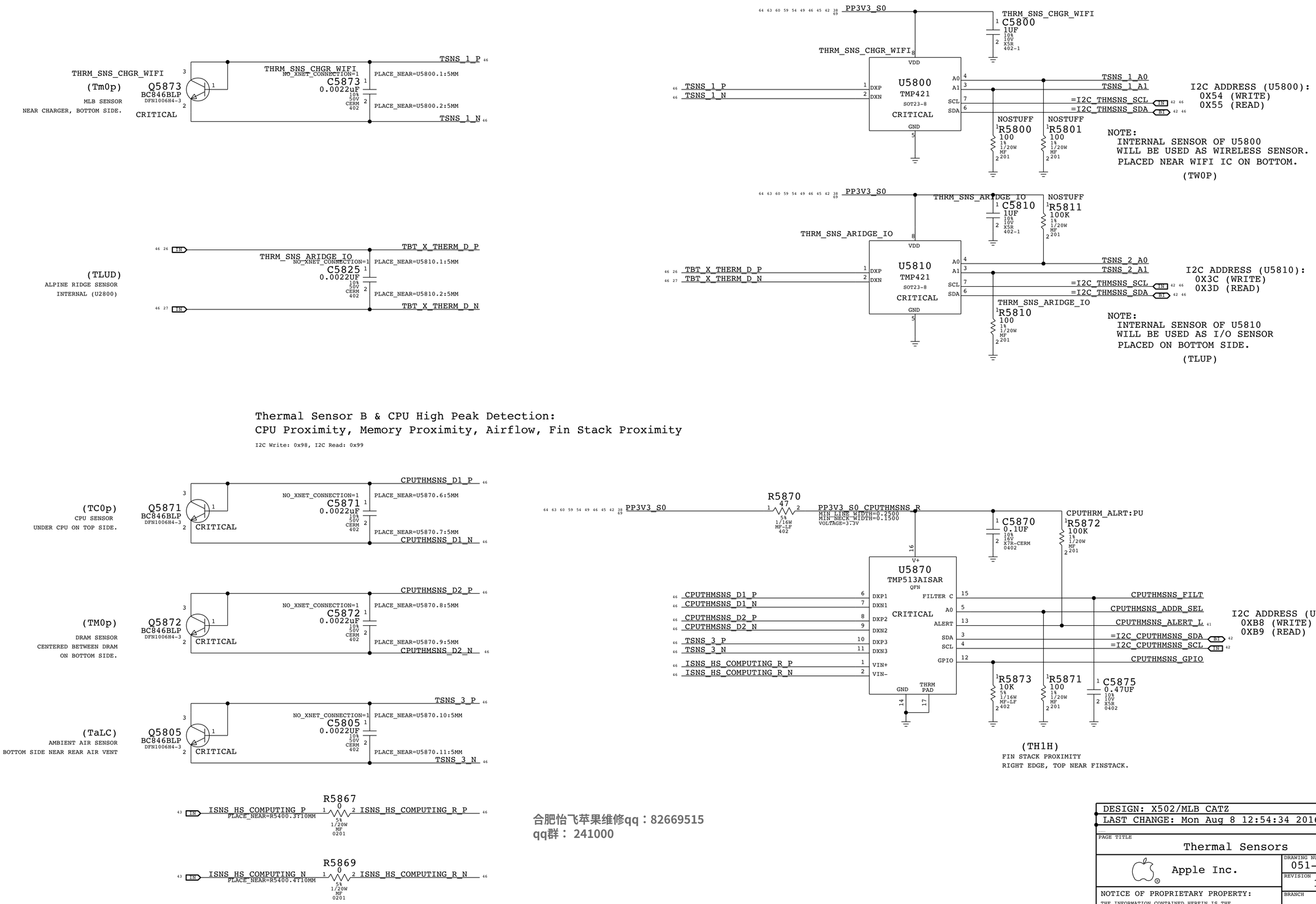

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BOM_COST_GROUP=SENSORS

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PAGE TITLE
Thermal Sensors

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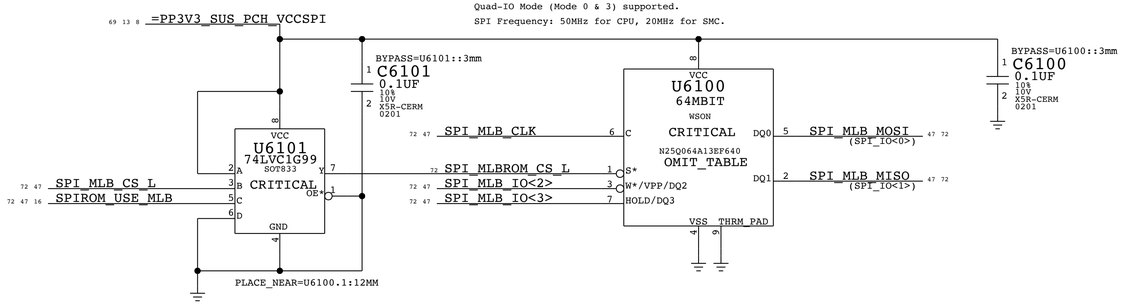
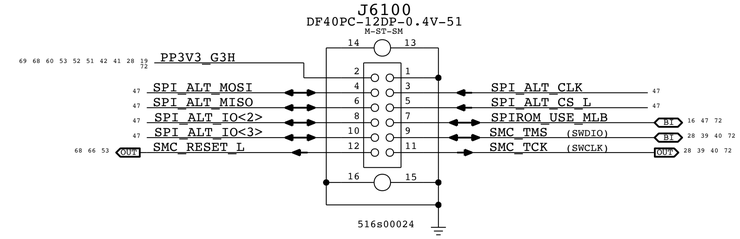
SPI ROM - Combo BGA Footprint (3 vendors)

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

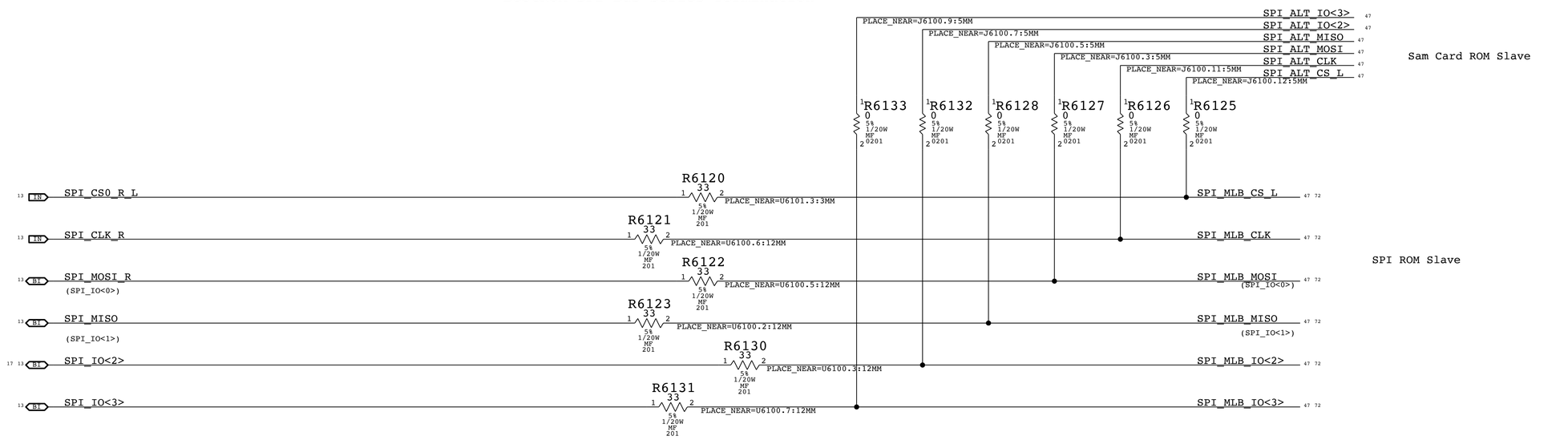


SPI+SWD SAM Connector

CRITICAL



BootROM SPI Bus Series Termination



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BOM_COST_GROUP=CPU SUPPORT

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PAGE TITLE
SPI ROM & SWD Debug

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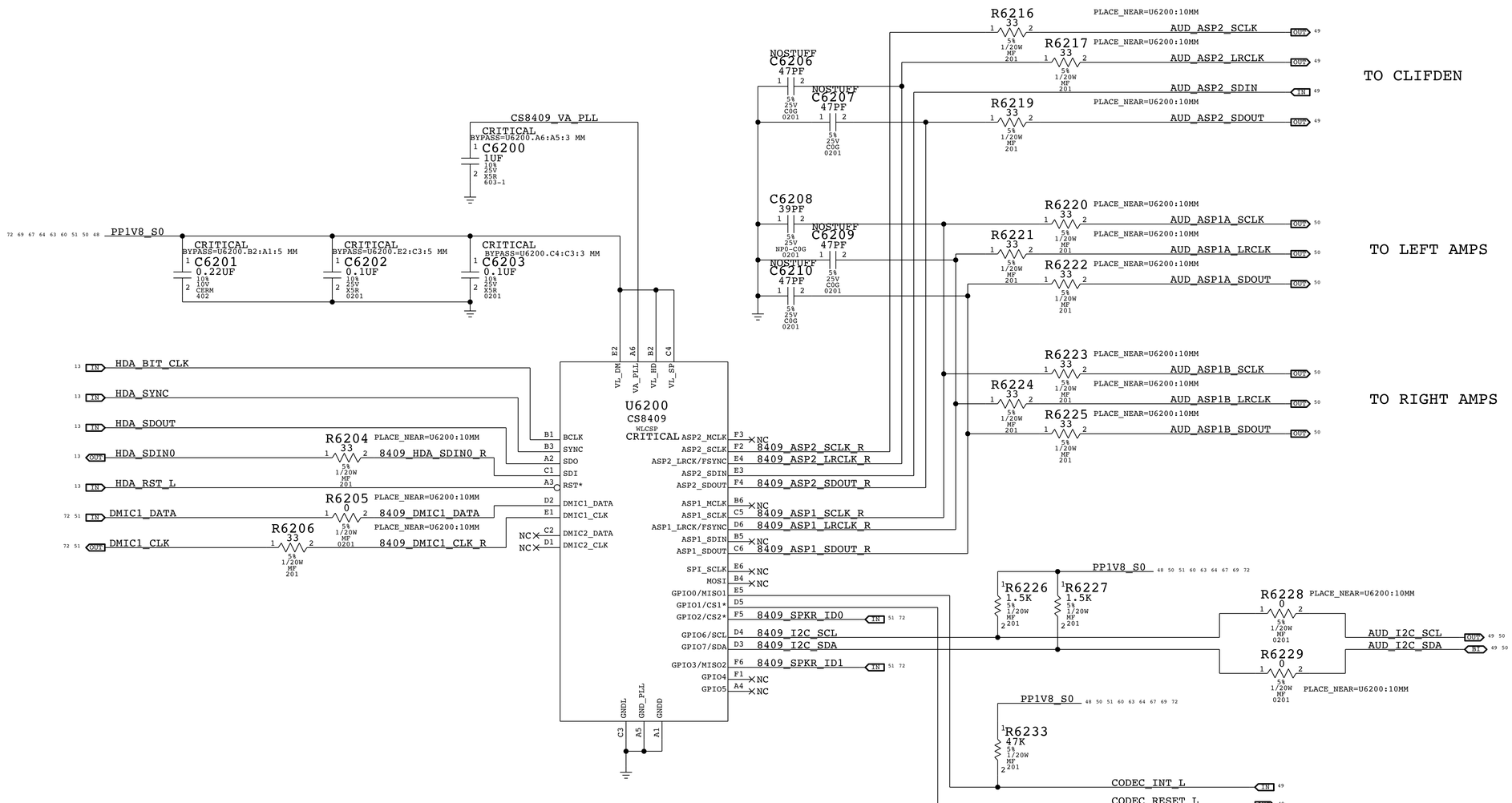

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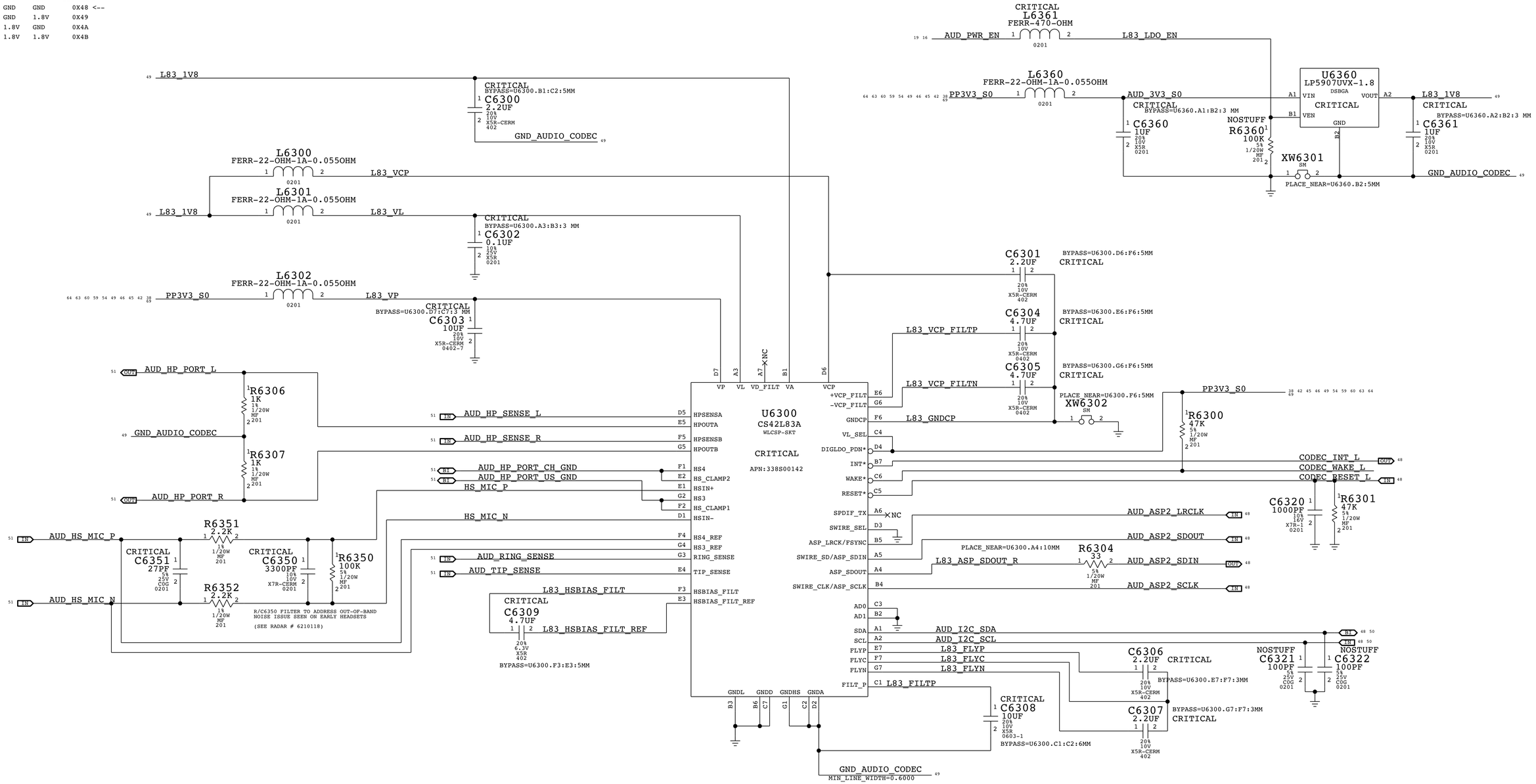
AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B



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BOM_COST_GROUP=AUDIO

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JACK CODEC

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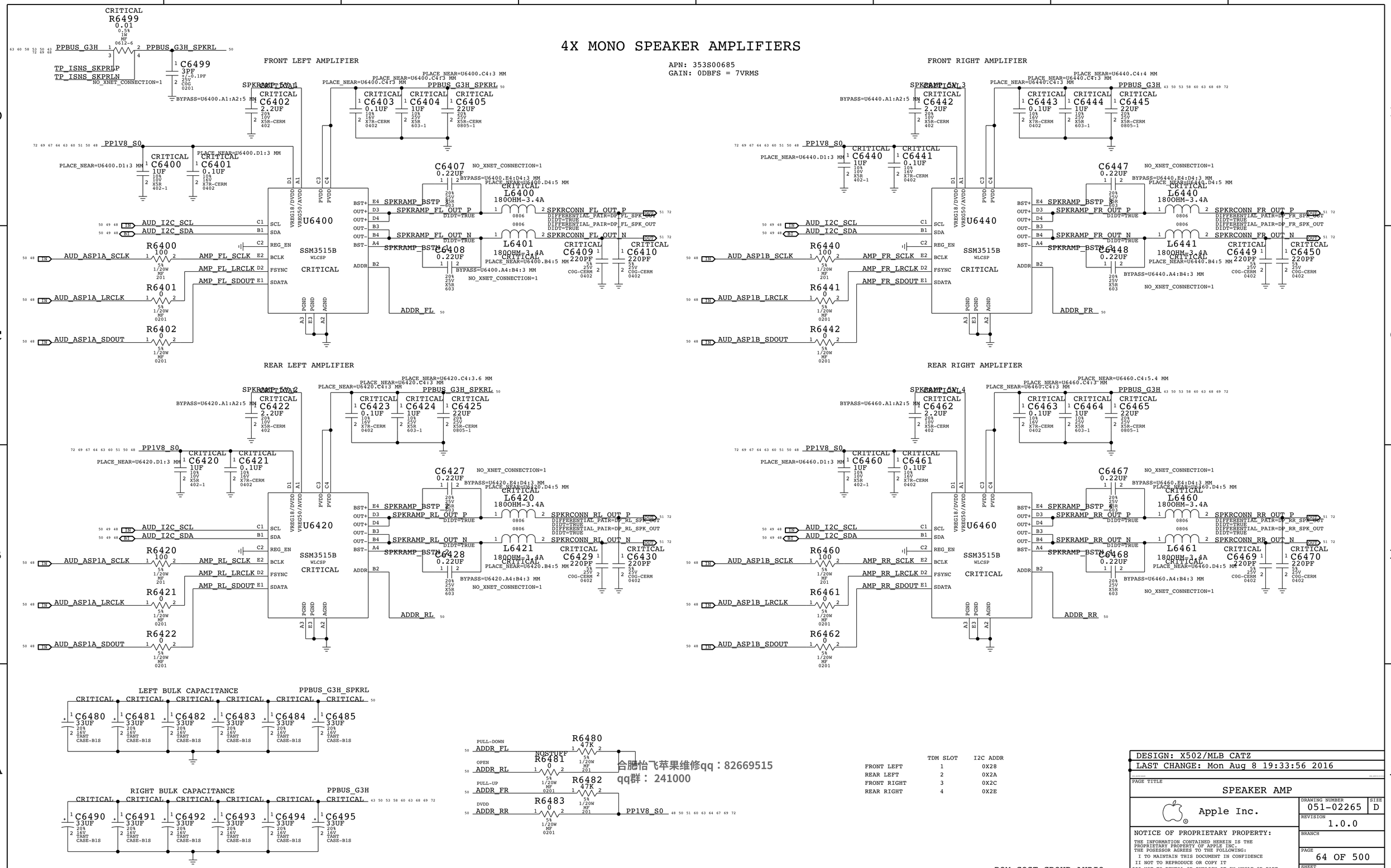
4X MONO SPEAKER AMPLIFIERS

APN: 353S00685
GAIN: 0DBFS = 7VRMS



	TDM SLOT	I2C ADDR
FRONT LEFT	1	0X28
REAR LEFT	2	0X2A
FRONT RIGHT	3	0X2C
REAR RIGHT	4	0X2E

BOM_COST_GROUP=AUDIO

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PAGE TITLE
SPEAKER AMP

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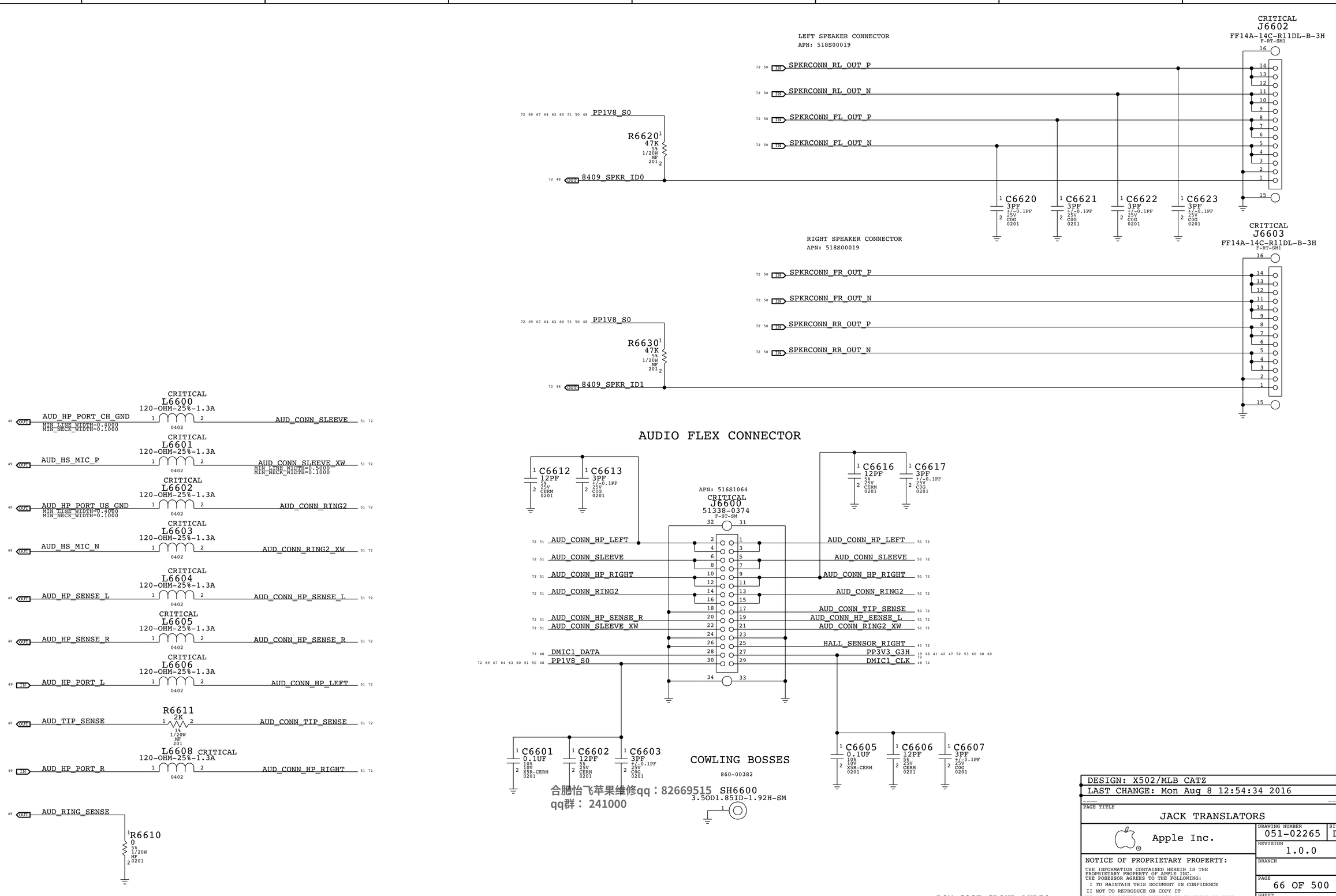

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PAGE TITLE
JACK TRANSLATORS

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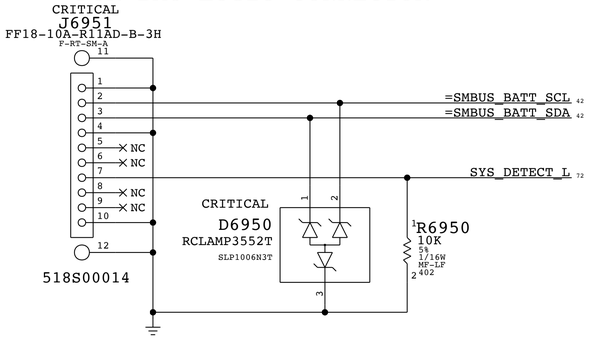
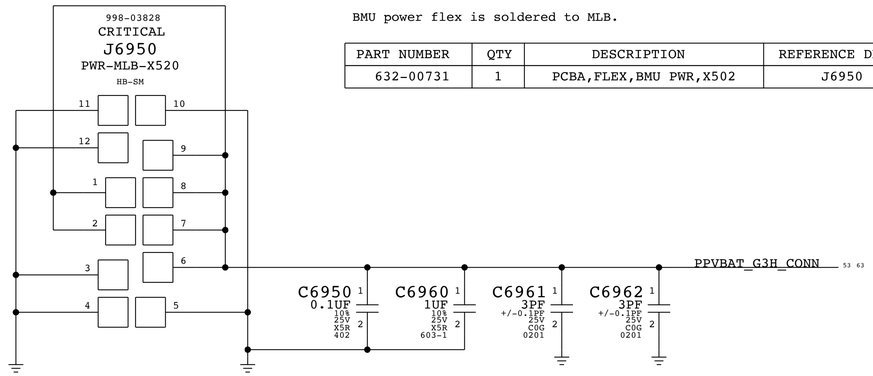
POR BMU LOGIC CONNECTOR



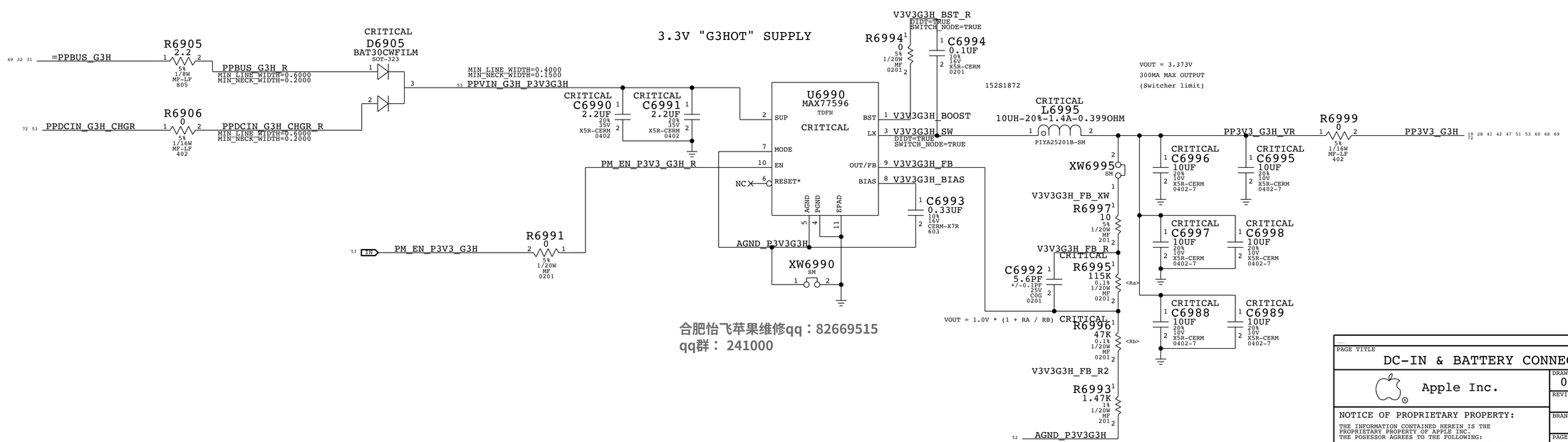
POR BATTERY (BMU) FLEX SOLDER PADS.



BMU power flex is soldered to MLB.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	

3.3V "G3HOT" SUPPLY



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PAGE TITLE
DC-IN & BATTERY CONNECTORS

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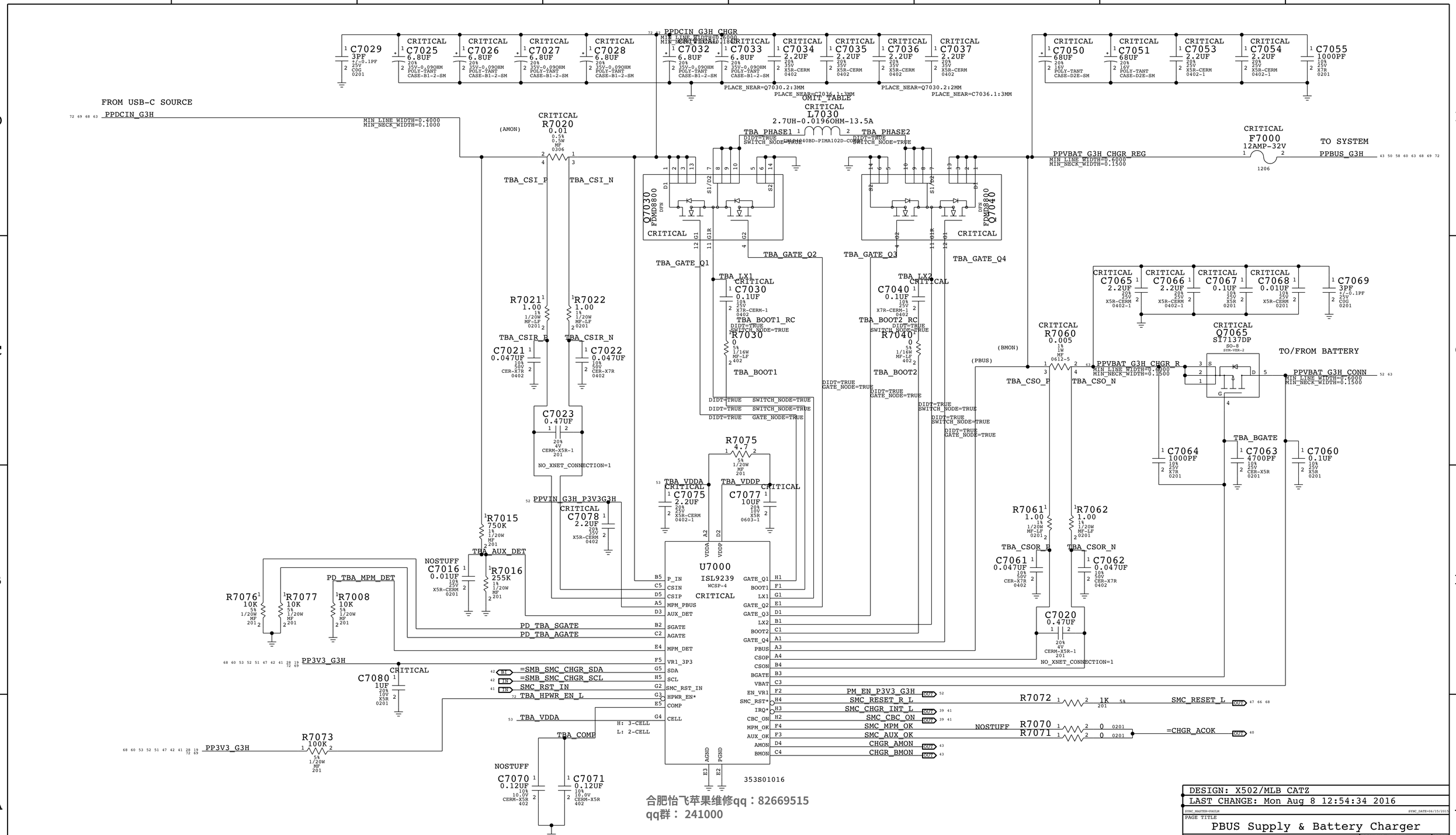

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

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PAGE TITLE
PBUS Supply & Battery Charger

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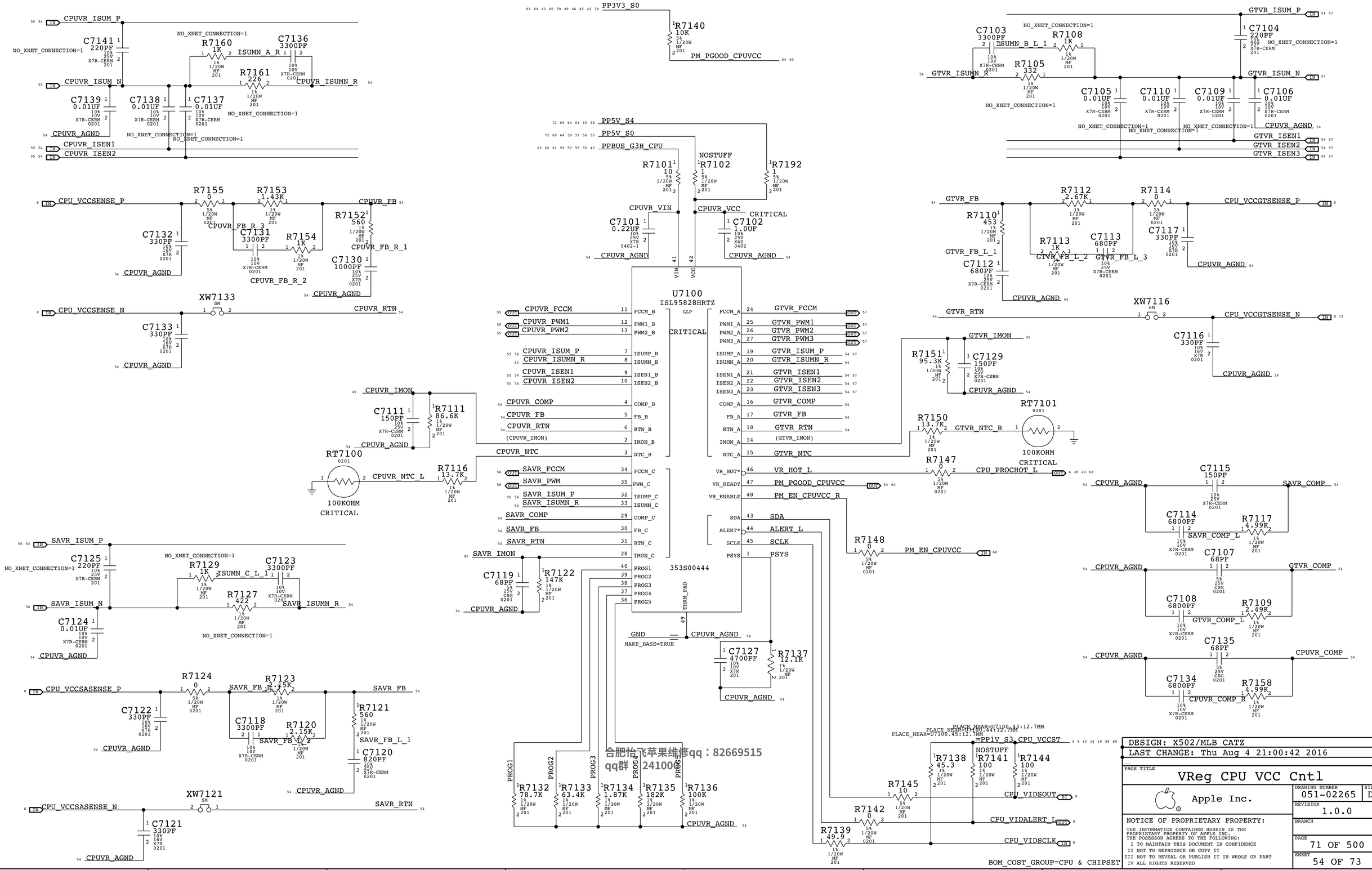
CPUVR_ISUM_P
C7141 220PF
NO_XNET_CONNECTION=1
R7160 1K
ISUMN_A_R
C7136 3300PF
R7161 226
CPUVR_ISUMN_R
CPUVR_ISUMN_N
C7139 0.01UF
C7138 0.01UF
C7137 0.01UF
CPUVR_AGND
CPUVR_ISEN1
CPUVR_ISEN2
PP3V3_S0
R7140 10K
PM_PGOOD_CPUVCC
GTVR_ISUM_P
C7104 220PF
C7103 3300PF
ISUMN_B_L_1
R7108 1K
R7105 332
GTVR_ISUMN_R
GTVR_ISUM_N
C7105 0.01UF
C7110 0.01UF
C7109 0.01UF
C7106 0.01UF
GTVR_ISEN1
GTVR_ISEN2
GTVR_ISEN3
PP5V_S4
PP5V_S0
PPBUS_G3H_CPU
R7101 10
NOSTUFF
R7102 1
R7192 1
CPUVR_VIN
CPUVR_VCC
CRITICAL
C7101 0.22UF
C7102 1.0UF
CPU_VCCSENSE_P
R7155 0
R7153 1.43K
CPUVR_FB
R7152 560
CPUVR_FB_R_3
C7131 3300PF
R7154 1K
CPUVR_FB_R_1
C7132 330PF
C7130 1000PF
CPUVR_FB_R_2
XW7133
CPU_VCCSENSE_N
CPUVR_RTN
C7133 330PF
U7100
ISL95828HRTZ
LLP
CPUVR_FCCM
CPUVR_PWM1
CPUVR_PWM2
CPUVR_ISUM_P
CPUVR_ISUMN_R
CPUVR_ISEN1
CPUVR_ISEN2
CPUVR_COMP
CPUVR_FB
CPUVR_RTN
(CPUVR_IMON)
CPUVR_NTC
SAVR_FCCM
SAVR_PWM
SAVR_ISUM_P
SAVR_ISUMN_R
SAVR_COMP
SAVR_FB
SAVR_RTN
SAVR_IMON
GTVR_FCCM
GTVR_PWM1
GTVR_PWM2
GTVR_PWM3
GTVR_ISUM_P
GTVR_ISUMN_R
GTVR_ISEN1
GTVR_ISEN2
GTVR_ISEN3
GTVR_COMP
GTVR_FB
GTVR_RTN
(GTVR_IMON)
GTVR_NTC
VR_HOT_L
PM_PGOOD_CPUVCC
PM_EN_CPUVCC_R
SDA
ALERT_L
SCLK
PSYS
CPU_PROCHOT_L
PM_EN_CPUVCC
353S00444
THRM_PAD
GND
MAKE_BASE=TRUE
C7127 4700PF
R7137 12.1K
GTVR_FB
R7112 2.67K
R7114 0
CPU_VCCGTSENSE_P
R7110 453
R7113 1K
C7113 680PF
C7117 330PF
GTVR_FB_L_1
GTVR_FB_L_2
GTVR_FB_L_3
C7112 680PF
GTVR_RTN
XW7116
CPU_VCCGTSENSE_N
C7116 330PF
GTVR_IMON
R7151 95.3K
C7129 150PF
RT7101
R7150 13.7K
GTVR_NTC_R
100KOHM
CRITICAL
R7147 0
C7115 150PF
SAVR_COMP
C7114 6800PF
R7117 4.99K
SAVR_COMP_L
C7107 68PF
GTVR_COMP
C7108 6800PF
R7109 2.49K
GTVR_COMP_L
C7135 68PF
CPUVR_COMP
C7134 6800PF
R7158 4.99K
CPUVR_COMP_R
R7148 0
PLACE_NEAR=U7100.43:12.7MM
PLACE_NEAR=U7100.44:12.7MM
PLACE_NEAR=U7100.45:12.7MM
=PP1V_S3
CPU_VCCST
NOSTUFF
R7138 45.3
R7141 100
R7144 100
R7145 10
R7142 0
R7139 49.9
CPU_VIDSOUT
CPU_VIDALERT_L
CPU_VIDSCLK
BOM_COST_GROUP=CPU & CHIPSET
CPUVR_IMON
C7111 150PF
R7111 86.6K
RT7100
CPUVR_NTC_L
R7116 13.7K
SAVR_ISUM_P
C7125 220PF
R7129 1K
ISUMN_C_L_1
C7123 3300PF
R7127 422
SAVR_ISUMN_R
SAVR_ISUMN_N
C7124 0.01UF
C7119 68PF
R7122 147K
CPU_VCCSASENSE_P
R7124 0
R7123 2.15K
SAVR_FB_R_1
SAVR_FB
C7122 330PF
C7118 3300PF
R7120 2.15K
R7121 560
SAVR_FB_L_1
C7120 820PF
XW7121
CPU_VCCSASENSE_N
SAVR_RTN
C7121 330PF
PROG1
PROG2
PROG3
PROG4
PROG5
R7132 78.7K
R7133 63.4K
R7134 1.87K
R7135 182K
R7136 100K
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qq群：241006
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VReg CPU VCC Cntl
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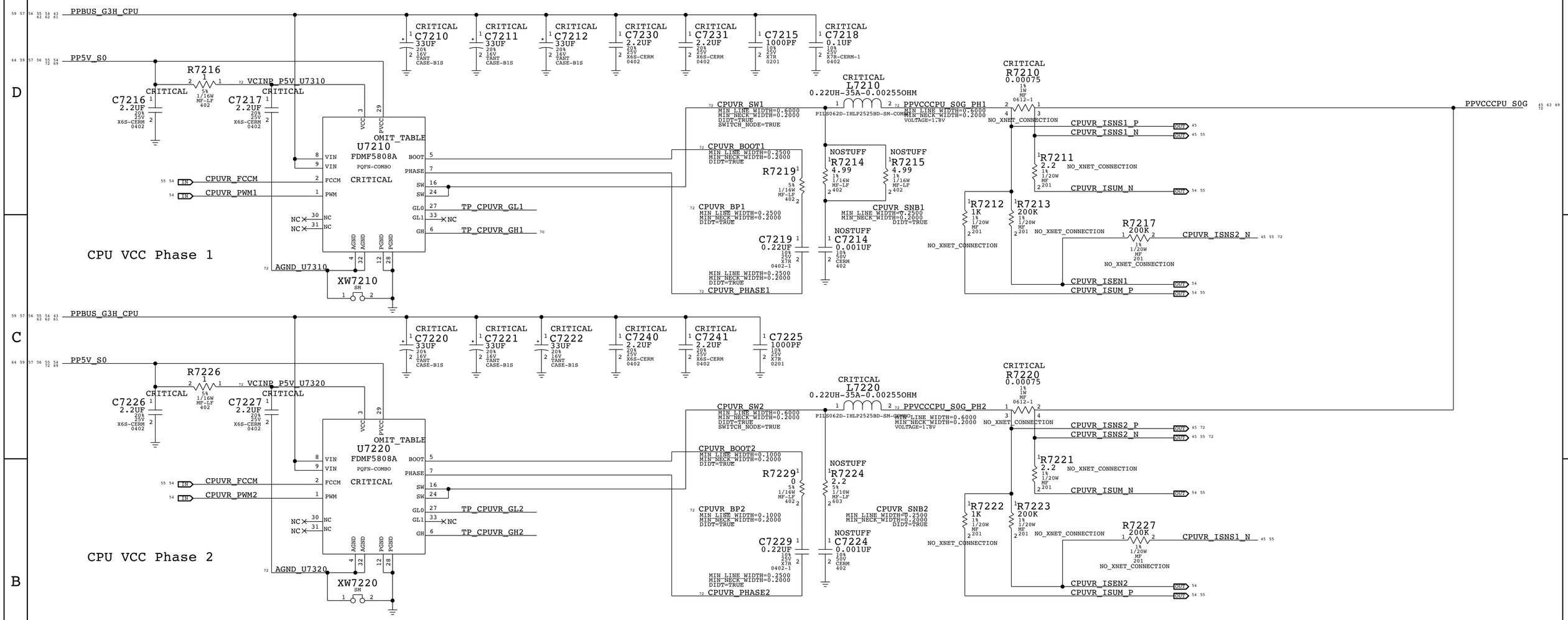

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	5	IC,SIC635,DR MOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7410,U7420,U7430	CRITICAL	

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qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

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PAGE TITLE
CPU IMVP VCC & VCCSA

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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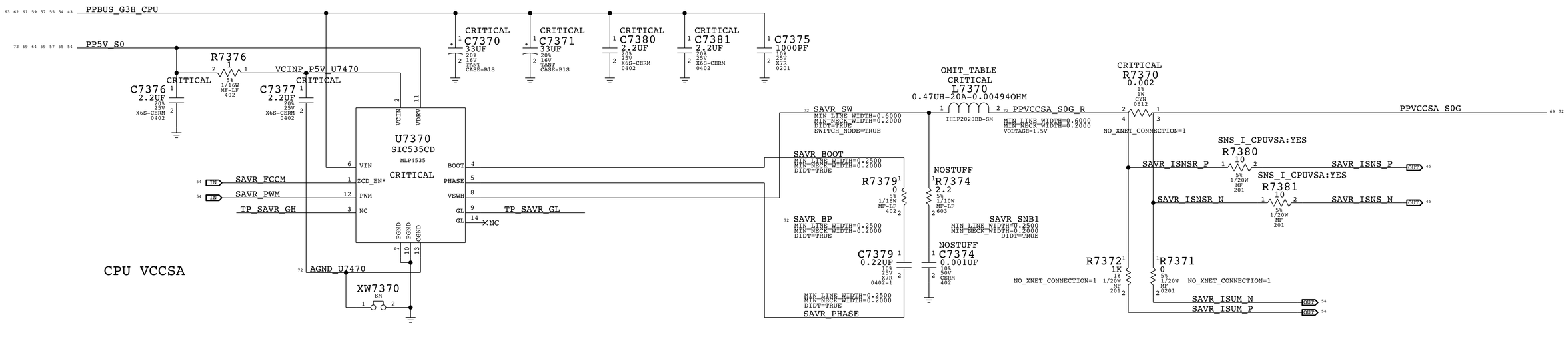

合肥怡飞苹果维修qq：82669515
qq群： 241000

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
IMVP VCCSA

Apple Inc.

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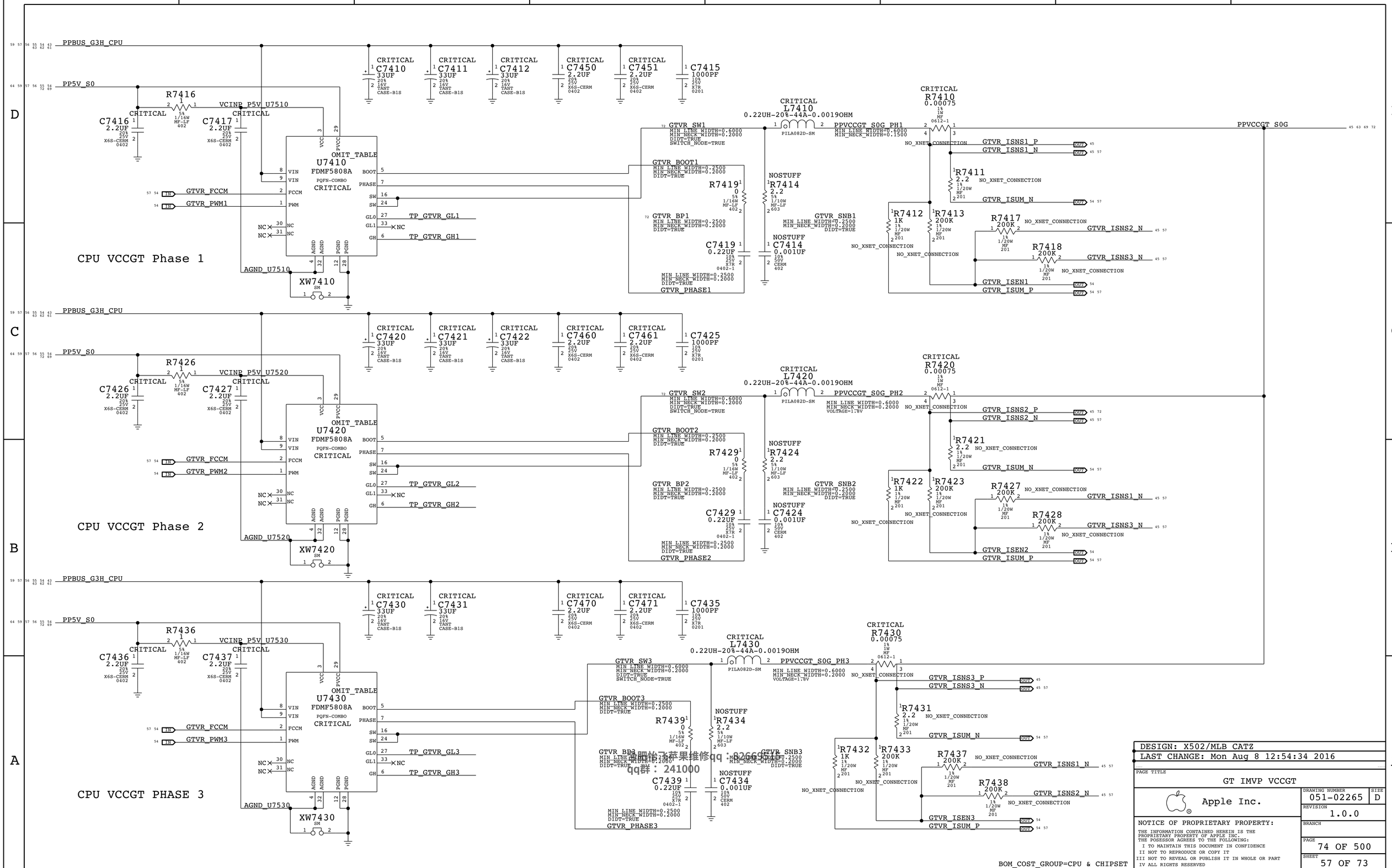

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qq群：241000

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LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
GT IMVP VCCGT

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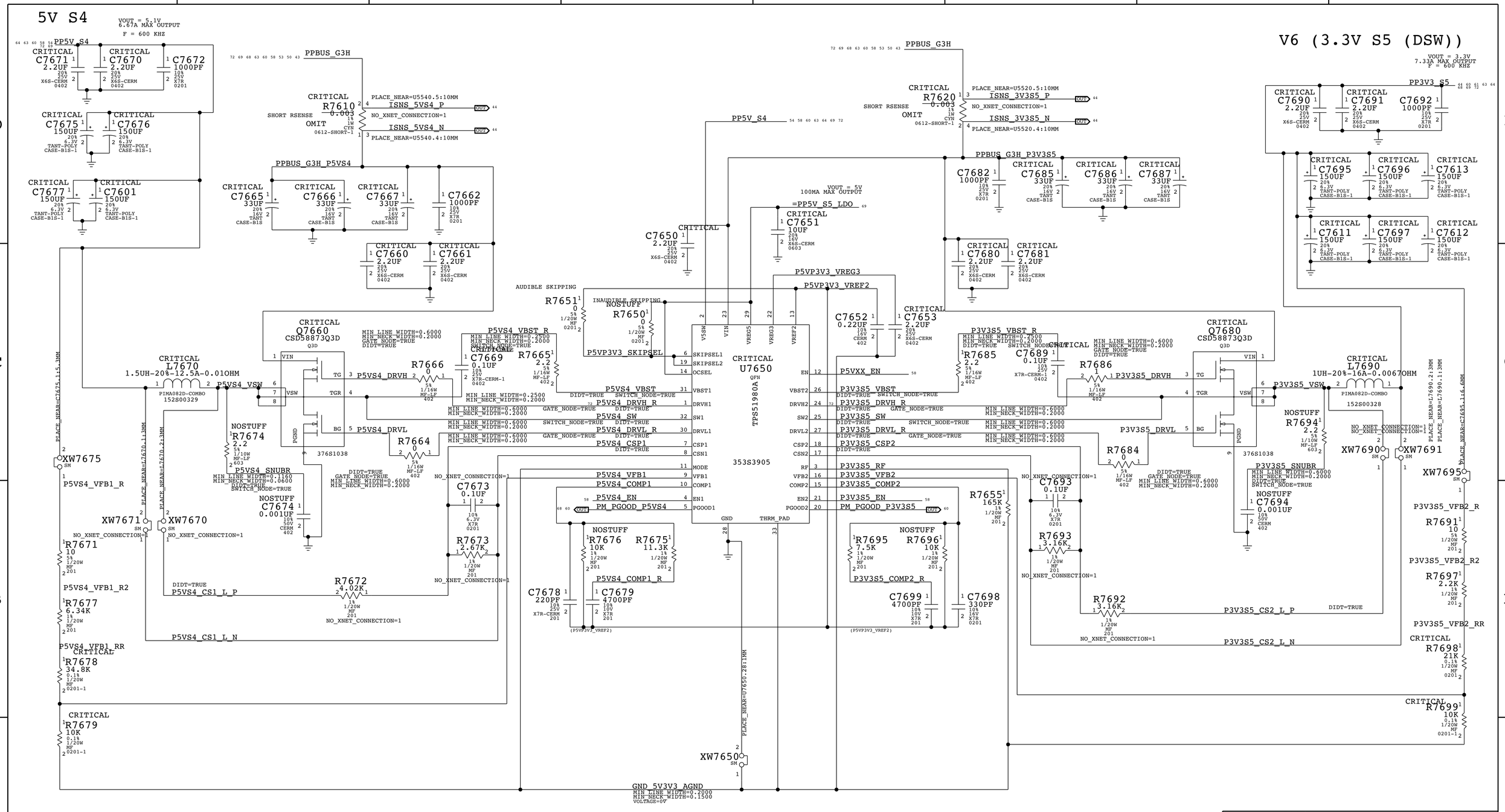

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BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
VR - 5V S4, 3.3V S5

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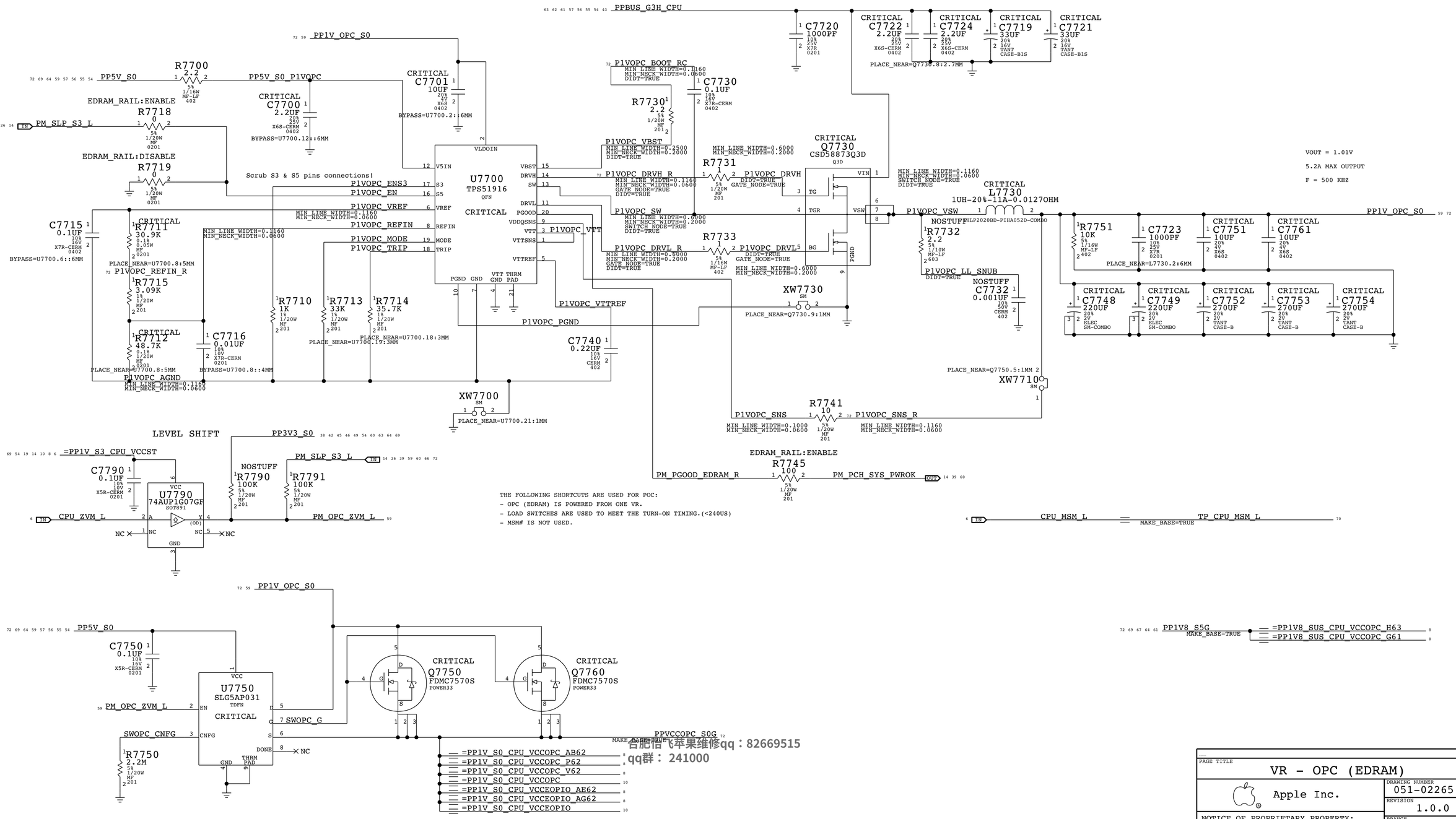
1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)



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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
VR - OPC (EDRAM)

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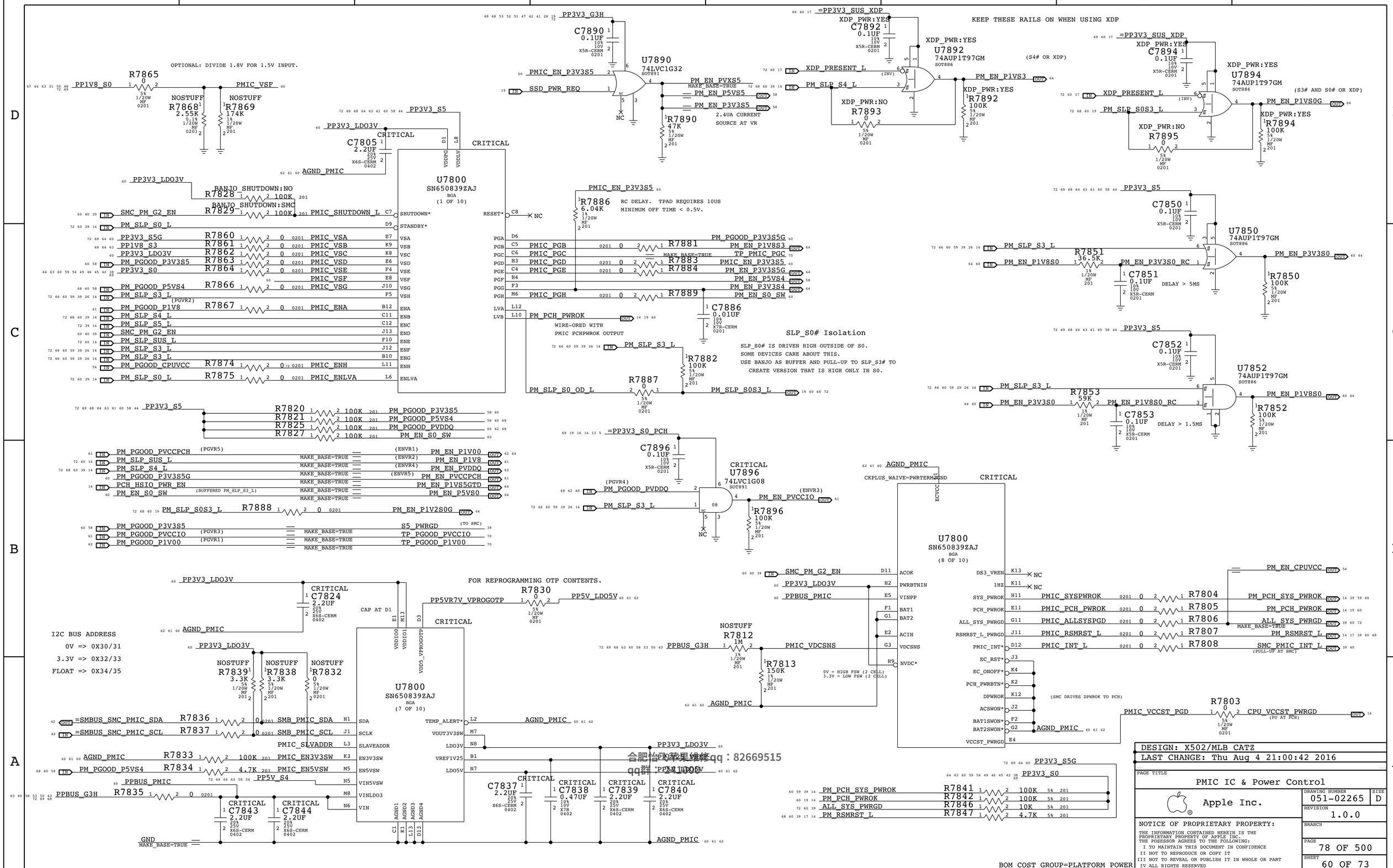
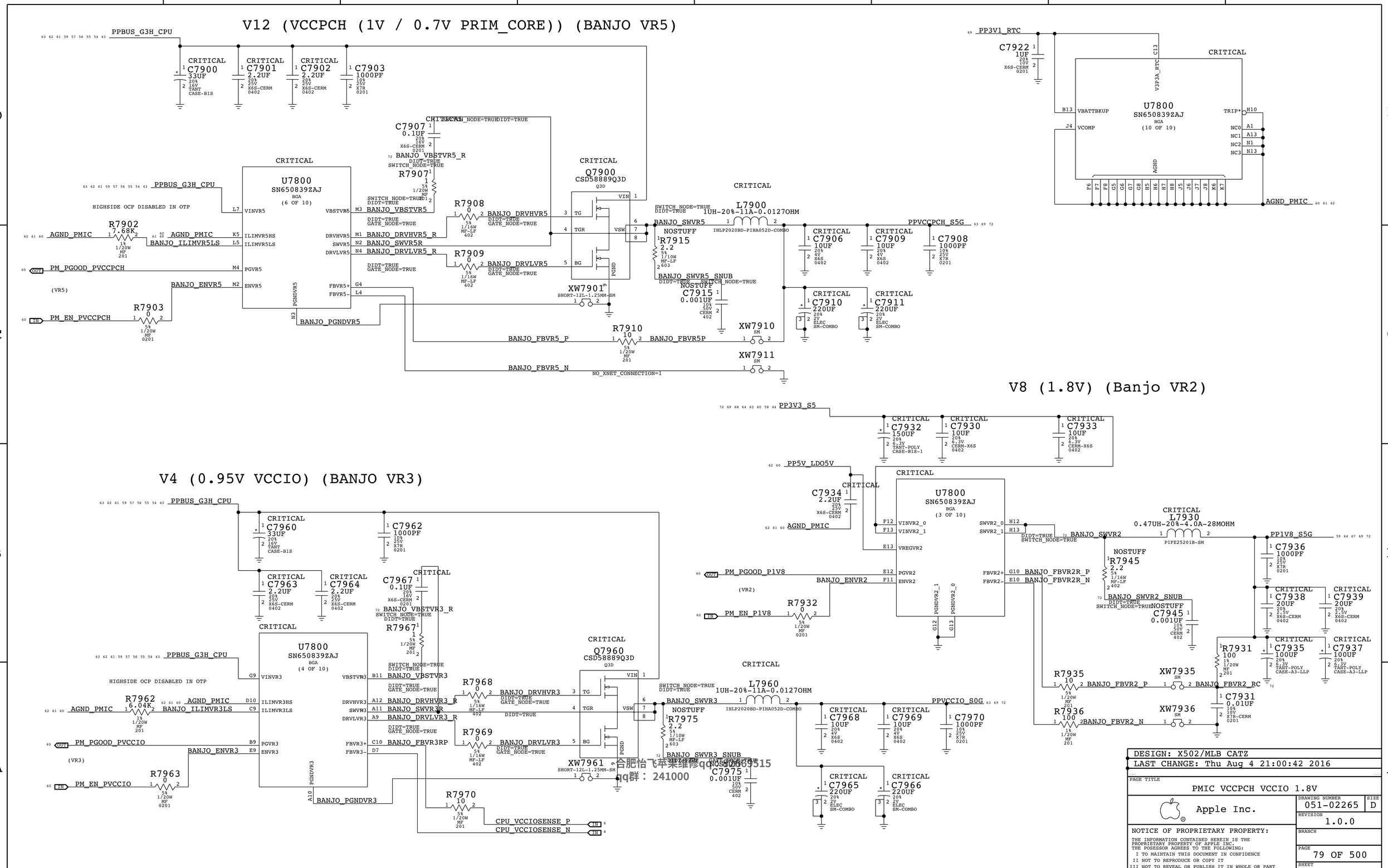


合肥怡天苹果维修 qq：82669515
qq群：291000



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DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PMIC VCCPCH VCCIO 1.8V

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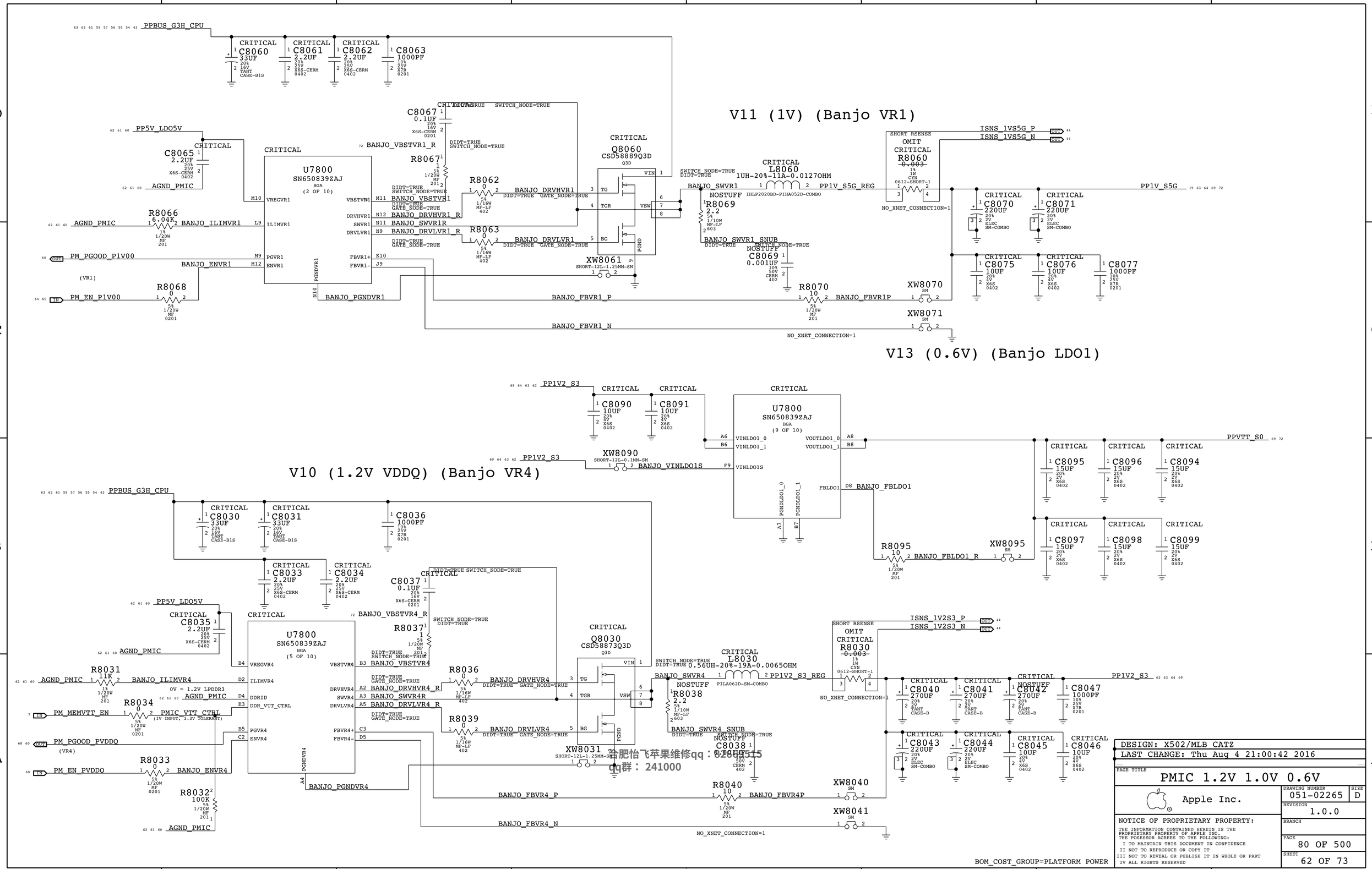
V11 (1V) (Banjo VR1)
V13 (0.6V) (Banjo LDO1)
V10 (1.2V VDDQ) (Banjo VR4)
U7800
SN650839ZAJ
BGA
(2 OF 10)
(9 OF 10)
(5 OF 10)
Q8060
CSD58889Q3D
Q8030
CSD58873Q3D
L8060
1UH-20%-11A-0.0127OHM
L8030
0.56UH-20%-19A-0.0065OHM
PPBUS_G3H_CPU
PP5V_LDO5V
AGND_PMIC
PM_PGOOD_P1V00
PM_EN_P1V00
PM_MEMVTT_EN
PM_PGOOD_PVDDO
PM_EN_PVDDO
PP1V2_S3
PPVTT_S0
PP1V_S5G
PP1V_S5G_REG
PP1V2_S3_REG
ISNS_1VS5G_P
ISNS_1VS5G_N
ISNS_1V2S3_P
ISNS_1V2S3_N
BANJO_SWVR1
BANJO_SWVR4
BANJO_FBVR1_P
BANJO_FBVR1_N
BANJO_FBVR4_P
BANJO_FBVR4_N
BANJO_FBVR1P
BANJO_FBVR4P
BANJO_FBLDO1
BANJO_FBLDO1_R
BANJO_VINLDO1S
BANJO_PGNDVR1
BANJO_PGNDVR4
BANJO_VBSTVR1_R
BANJO_VBSTVR4_R
BANJO_ILIMVR1
BANJO_ILIMVR4
BANJO_ENVR1
BANJO_ENVR4
BANJO_DRVHVR1
BANJO_DRVLVR1
BANJO_DRVHVR1_R
BANJO_DRVLVR1_R
BANJO_SWVR1R
BANJO_SWVR4R
BANJO_DRVHVR4
BANJO_DRVLVR4
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BANJO_SWVR1_SNUB
BANJO_SWVR4_SNUB
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BOM_COST_GROUP=PLATFORM_POWER
DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016
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PMIC 1.2V 1.0V 0.6V
Apple Inc.
DRAWING NUMBER 051-02265
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69 64 63 62 PP1V2_S3	C8100 12PF 5% 25V CERM 0201	CRITICAL	C8101 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8102 3PF +/-0.1PF 25V C0G 0201		C8103 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8104 3PF +/-0.1PF 25V C0G 0201		C8105 3PF +/-0.1PF 25V C0G 0201
69 64 63 60 PP1V8_S3	C8106 3PF +/-0.1PF 25V C0G 0201		C8107 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8108 3PF +/-0.1PF 25V C0G 0201		C8109 3.5PF +/-0.25PF 25V C0G 0201
72 69 68 64 63 61 60 58 44 PP3V3_S5	C8110 12PF 5% 25V CERM 0201		C8111 3PF +/-0.1PF 25V C0G 0201
72 69 64 63 60 58 54 PP5V_S4	C8112 12PF 5% 25V CERM 0201		C8113 3.5PF +/-0.25PF 25V C0G 0201
72 69 64 63 60 58 54 PP5V_S4	C8114 3.5PF +/-0.25PF 25V C0G 0201		C8115 3.5PF +/-0.25PF 25V C0G 0201
72 69 64 63 60 58 54 PP5V_S4	C8116 12PF 5% 25V CERM 0201		C8117 3PF +/-0.1PF 25V C0G 0201
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8118 3PF +/-0.1PF 25V C0G 0201		C8119 3PF +/-0.1PF 25V C0G 0201
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8120 3PF +/-0.1PF 25V C0G 0201		C8121 3.5PF +/-0.25PF 25V C0G 0201
72 69 68 53 PPDCIN_G3H	C8122 12PF 5% 25V CERM 0201		C8123 3PF +/-0.1PF 25V C0G 0201
63 53 PPVBAT_G3H_CHGR_R	C8124 3PF +/-0.1PF 25V C0G 0201		C8125 3PF +/-0.1PF 25V C0G 0201
63 53 PPVBAT_G3H_CHGR_R	C8126 3PF +/-0.1PF 25V C0G 0201		C8127 3PF +/-0.1PF 25V C0G 0201
63 53 52 PPVBAT_G3H_CONN	C8128 12PF 5% 25V CERM 0201		C8129 3PF +/-0.1PF 25V C0G 0201
63 53 52 PPVBAT_G3H_CONN	C8130 3PF +/-0.1PF 25V C0G 0201		C8131 3PF +/-0.1PF 25V C0G 0201
72 69 55 45 PPVCCCPU_S0G	C8132 3PF +/-0.1PF 25V C0G 0201		C8133 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 60 51 50 48 PP1V8_S0	C8134 12PF 5% 25V CERM 0201	FREQUENCY SPECIFIC CRITICAL	C8135 3.0PF +/-0.1PF 25V NPO-COG 0201
72 69 64 63 62 19 PP1V_S5G	C8137 3PF +/-0.1PF 25V C0G 0201		
72 69 64 63 62 19 PP1V_S5G	C8138 3PF +/-0.1PF 25V C0G 0201	NOSTUFF	
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8136 3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 45 44 43 41 72 69 PP3V3_S4	C8139 3PF +/-0.1PF 25V C0G 0201	NOSTUFF	
69 64 63 62 PP1V2_S3	C8140 12PF 5% 25V CERM 0201	NOSTUFF	C8141 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8142 12PF 5% 25V CERM 0201	NOSTUFF	C8143 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8144 12PF 5% 25V CERM 0201	NOSTUFF	C8145 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8146 12PF 5% 25V CERM 0201	NOSTUFF	C8147 3PF +/-0.1PF 25V C0G 0201
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8148 12PF 5% 25V CERM 0201		C8149 3PF +/-0.1PF 25V C0G 0201
69 64 63 60 PP1V8_S3	C8150 12PF 5% 25V CERM 0201	NOSTUFF	C8151 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8152 3PF +/-0.1PF 25V C0G 0201		C8153 3PF +/-0.1PF 25V C0G 0201
69 64 63 60 PP1V8_S3	C8155 3PF +/-0.1PF 25V C0G 0201		
67 PPBUS_SSD_FLT	C8157 3.5PF +/-0.25PF 25V C0G 0201		
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8158 3PF +/-0.1PF 25V C0G 0201		C8159 3PF +/-0.1PF 25V C0G 0201
69 64 63 PP5V_S5	C8154 3PF +/-0.1PF 25V C0G 0201		
69 64 63 PP5V_S5	C8156 3PF +/-0.1PF 25V C0G 0201		
63 28 27 PP3V3_TBT_X_LC	C8160 12PF 5% 25V CERM 0201		C8161 3PF +/-0.1PF 25V C0G 0201
63 28 27 PP3V3_TBT_X_LC	C8162 12PF 5% 25V CERM 0201		C8163 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8164 3PF +/-0.1PF 25V C0G 0201		C8165 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8166 12PF 5% 25V CERM 0201		C8167 3PF +/-0.1PF 25V C0G 0201
28 PP3V3_TBT_X_S0	C8168 12PF 5% 25V CERM 0201		C8169 3PF +/-0.1PF 25V C0G 0201
72 69 61 PPVCCPCH_S5G	C8170 3PF +/-0.1PF 25V C0G 0201		C8171 3PF +/-0.1PF 25V C0G 0201
72 69 63 57 45 PPVCCGT_S0G	C8172 3PF +/-0.1PF 25V C0G 0201		C8173 3PF +/-0.1PF 25V C0G 0201
72 69 61 PPVCCIO_S0G	C8175 3PF +/-0.1PF 25V C0G 0201		
69 30 28 PP3V3_UPC_XB_LDO	C8176 12PF 5% 25V CERM 0201		C8177 3PF +/-0.1PF 25V C0G 0201
72 69 68 64 63 61 60 58 44 PP3V3_S5	C8178 12PF 5% 25V CERM 0201		C8179 3PF +/-0.1PF 25V C0G 0201
69 PP3V3_S5_SSD_SNS	C8174 3.5PF +/-0.25PF 25V C0G 0201		
72 69 63 57 45 PPVCCGT_S0G	C8181 3PF +/-0.1PF 25V C0G 0201		
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8182 3PF +/-0.1PF 25V C0G 0201		C8183 3PF +/-0.1PF 25V C0G 0201
69 64 63 62 PP1V2_S3	C8185 3PF +/-0.1PF 25V C0G 0201		
72 69 68 60 58 53 50 43 PPBUS_G3H	C8187 3PF +/-0.1PF 25V C0G 0201		
27 PP0V9_TBT_X_SVR	C8188 12PF 5% 25V CERM 0201		C8189 3PF +/-0.1PF 25V C0G 0201
72 69 68 64 63 61 60 58 44 PP3V3_S5	C8180 3PF +/-0.1PF 25V C0G 0201		
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8191 3PF +/-0.1PF 25V C0G 0201		
72 69 64 63 60 58 54 PP5V_S4	C8192 12PF 5% 25V CERM 0201		C8193 3PF +/-0.1PF 25V C0G 0201
72 69 64 63 60 58 54 PP5V_S4	C8194 12PF 5% 25V CERM 0201		C8195 3PF +/-0.1PF 25V C0G 0201
72 69 64 63 60 58 54 PP5V_S4	C8197 3PF +/-0.1PF 25V C0G 0201		
69 64 63 PP5V_S5	C8199 3PF +/-0.1PF 25V C0G 0201		
72 69 64 63 60 58 54 PP5V_S4	C8196 12PF 5% 25V CERM 0201		C8198 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 60 51 50 48 PP1V8_S0	C81A0 2.9PF +/-0.05PF 25V C0G-CERM 0201	CRITICAL	C81A1 2.9PF +/-0.05PF 25V C0G-CERM 0201 CRITICAL
72 69 67 64 63 60 51 50 48 PP1V8_S0	C81A3 2.9PF +/-0.05PF 25V C0G-CERM 0201		
72 69 67 64 63 45 44 43 41 PP3V3_S4	C81A5 3.5PF +/-0.25PF 25V C0G 0201		
72 69 44 PP3V3_S4_WLS	C81A7 3PF +/-0.1PF 25V C0G 0201		
69 64 60 59 54 49 46 45 42 38 PP3V3_S0	C81A8 3PF +/-0.1PF 25V C0G 0201	NOSTUFF	C81A9 3PF +/-0.1PF 25V C0G 0201 NOSTUFF

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BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
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PAGE TITLE
RAIL DESENSE CAPS

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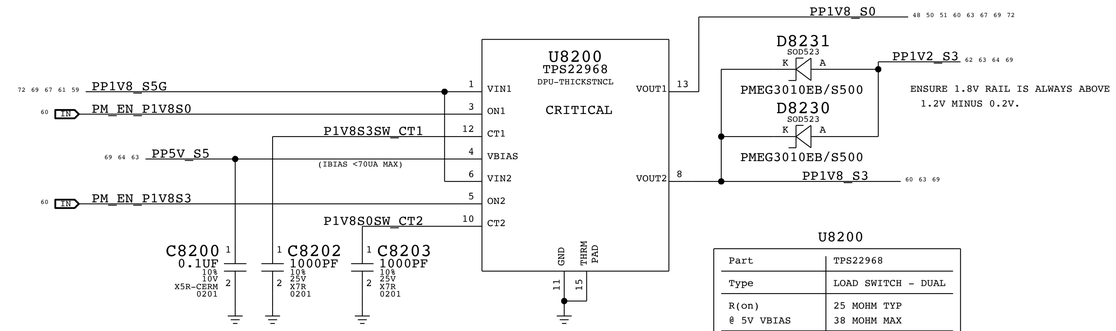
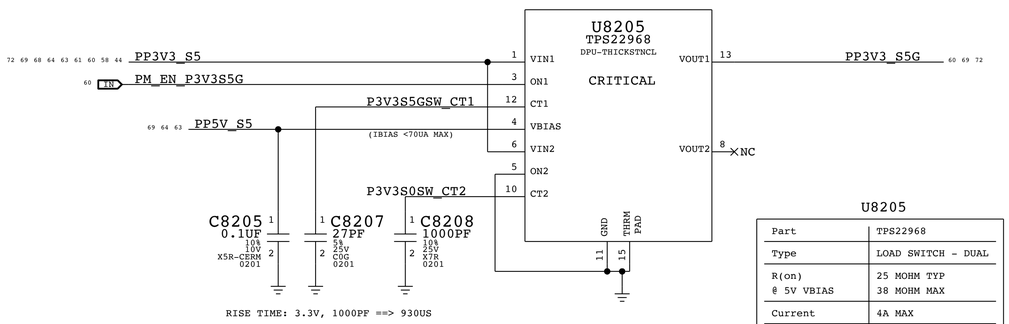


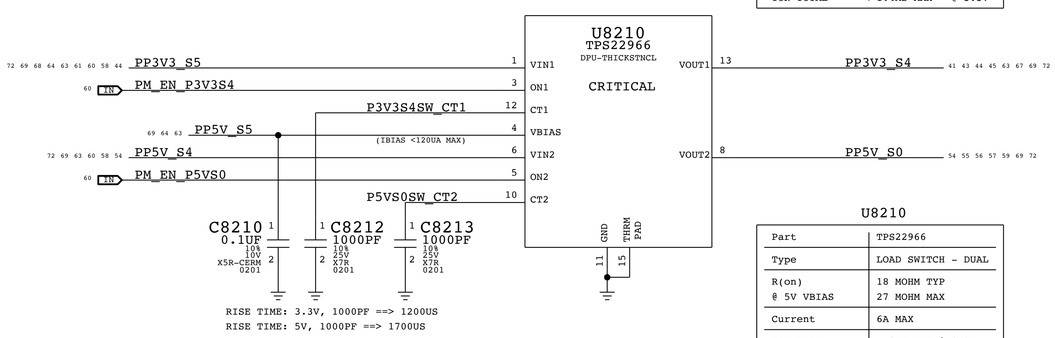
U8200

Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1MS MAX @ 1.8V



U8205

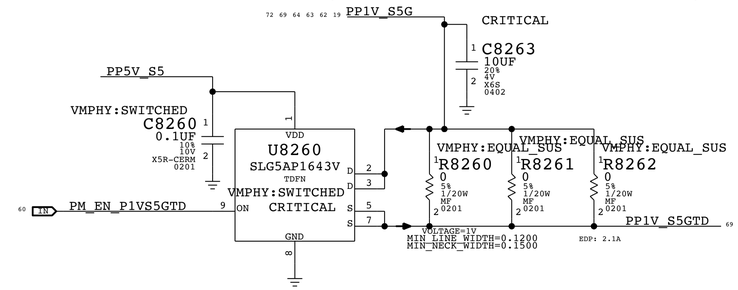
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1.4MS MAX @ 3.3V



U8210

Part	TPS22966
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	18 MOHM TYP 27 MOHM MAX
Current	6A MAX
TON-TOTAL	1.7MS MAX @ 3,3V 2.4MS MAX @ 5V

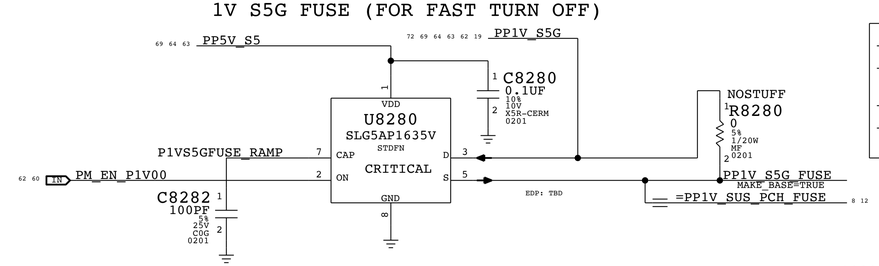
1V S5GTD SWITCH (VCCMPHYGT,VCCSRAM,VCCAPLLEBB)



U8260

Part	SLG5AP1643V
Type	Load Switch
R(on) @ 25C R(on) @ 70C	7.4 MOHM TYP 10.6 MOHM MAX
Current	6A MAX
TON-TOTAL	65US MAX @ 1V

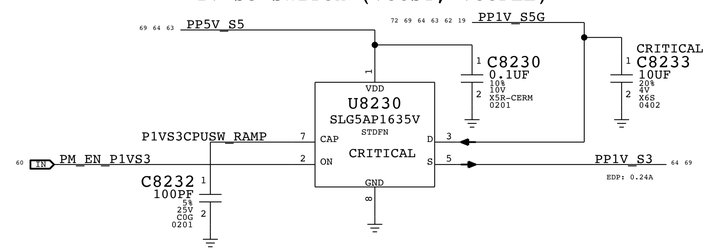
1V S5G FUSE (FOR FAST TURN OFF)



U8230

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V S3 SWITCH (VCCST, VCCPLL)

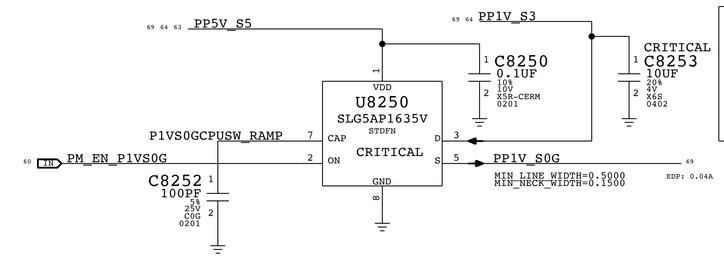


U8230

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

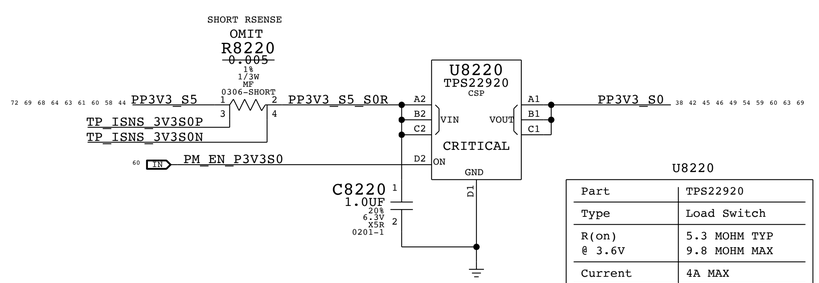
1V S0G CPU SWITCH (VCCSTG)

FAST TURN ON: < 64US



U8250

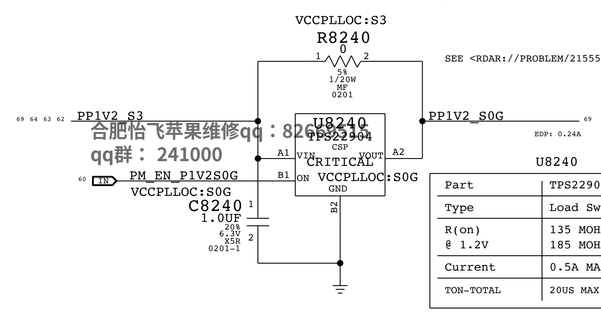
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V



U8220

Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.3 MOHM TYP 9.8 MOHM MAX
Current	4A MAX
TON-TOTAL	1.3MS MAX @ 3.6V

1V2 S0G SWITCH (VCCPLL_OC)



合肥怡飞苹果维修qq：826
qq群： 241000

U8240

Part	TPS22904
Type	Load Switch
R(on) @ 1.2V	135 MOHM TYP 185 MOHM MAX
Current	0.5A MAX
TON-TOTAL	20US MAX @ 1.2V

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
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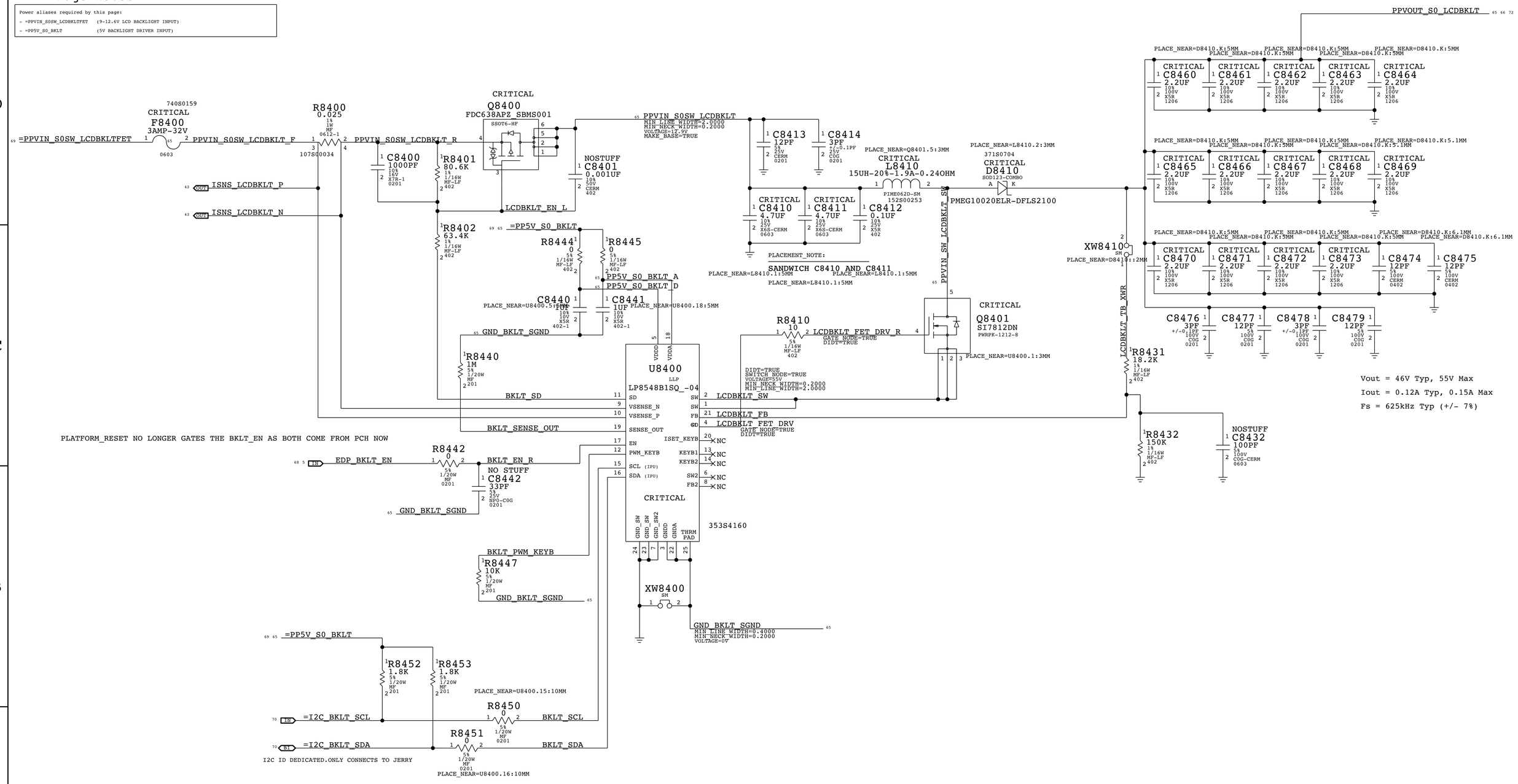
Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



LINE WIDTHS

PP5V_S0_BKLT_A
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

PP5V_S0_BKLT_D
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

PBUS LINE WIDTHS

PPVIN_S0SW_LCDBKLT_F
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_R
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V
GATE_NODE=TRUE DIDT=TRUE

PPVIN_SW_LCDBKLT_SW
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V
SWITCH_NODE=TRUE DIDT=TRUE

PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V

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qq群：24[illegible]

BOM_COST_GROUP=DISPLAY

PAGE TITLE
LCD Backlight Driver

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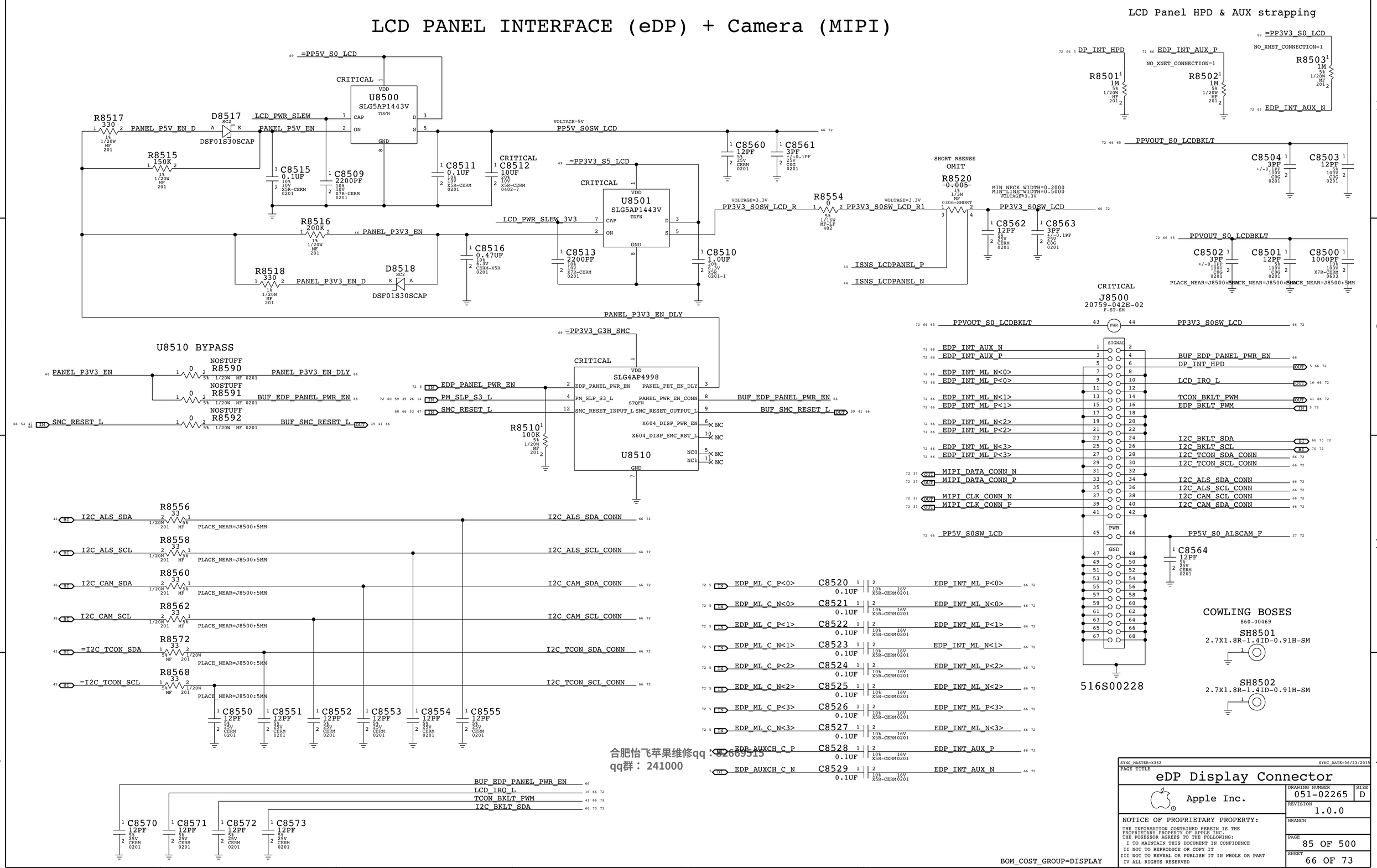
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



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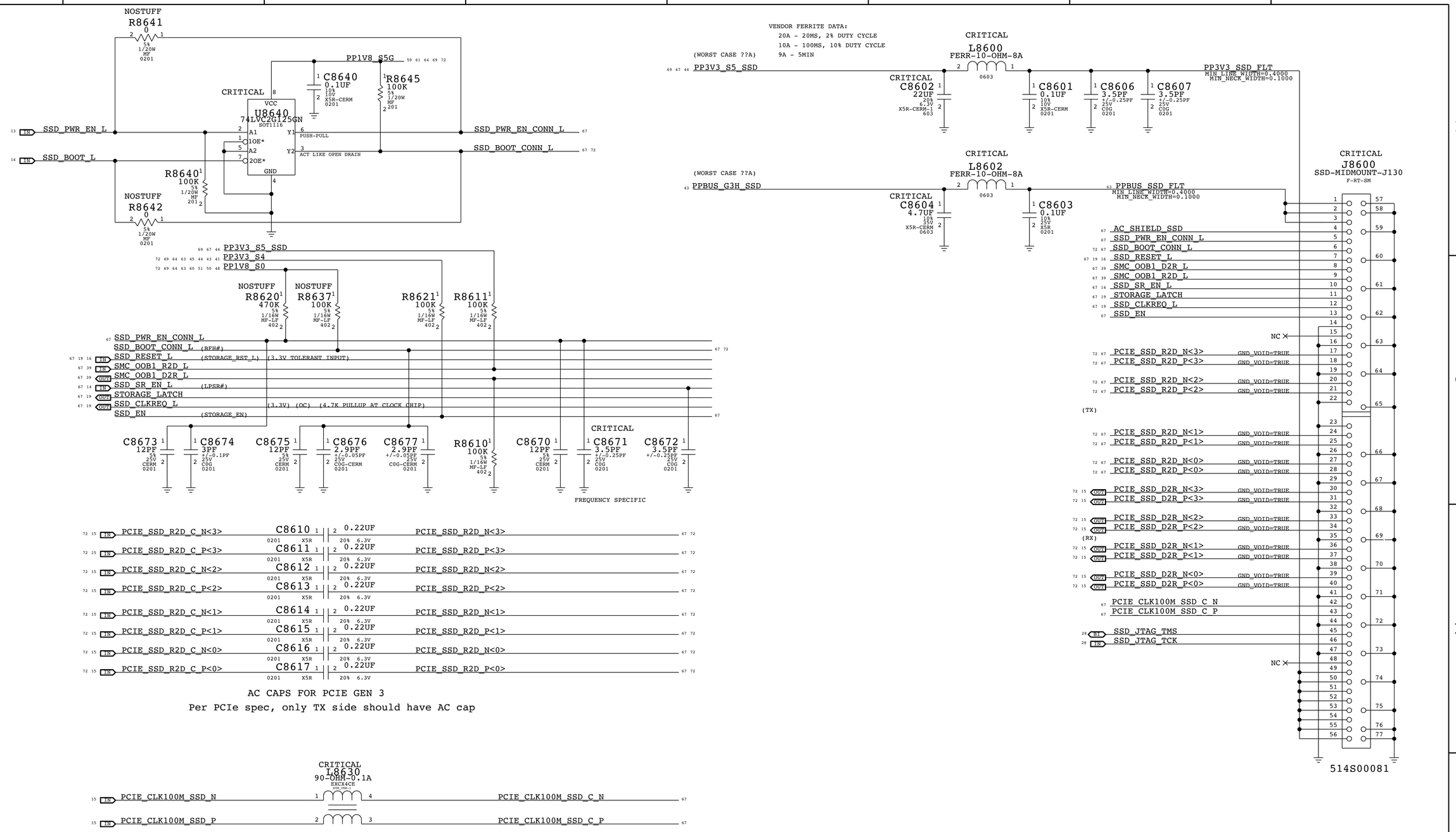
qq群： 241000



NOTES:

1. POWER-ON TO PERST_L DE-ASSERTION = 10MS MINIMUM
2. PP3V3_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF. (PIN 47, PP3V3_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
3. PCIE CLK100M ARE 2.5V SIGNALS.
4. OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.

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qq群：2[illegible]

SSD STANDOFFS

860-00380

SH8600 4.0OD1.6ID-0.85H-TH

SH8601 4.0OD1.6ID-0.85H-TH

DESIGN: X502/MLB CATZ	
LAST CHANGE: Thu Aug 4 21:00:42 2016	
PAGE TITLE: SSD MODULE	
Apple Inc.	DRAWING NUMBER: 051-02265 SIZE: D
	REVISION: 1.0.0
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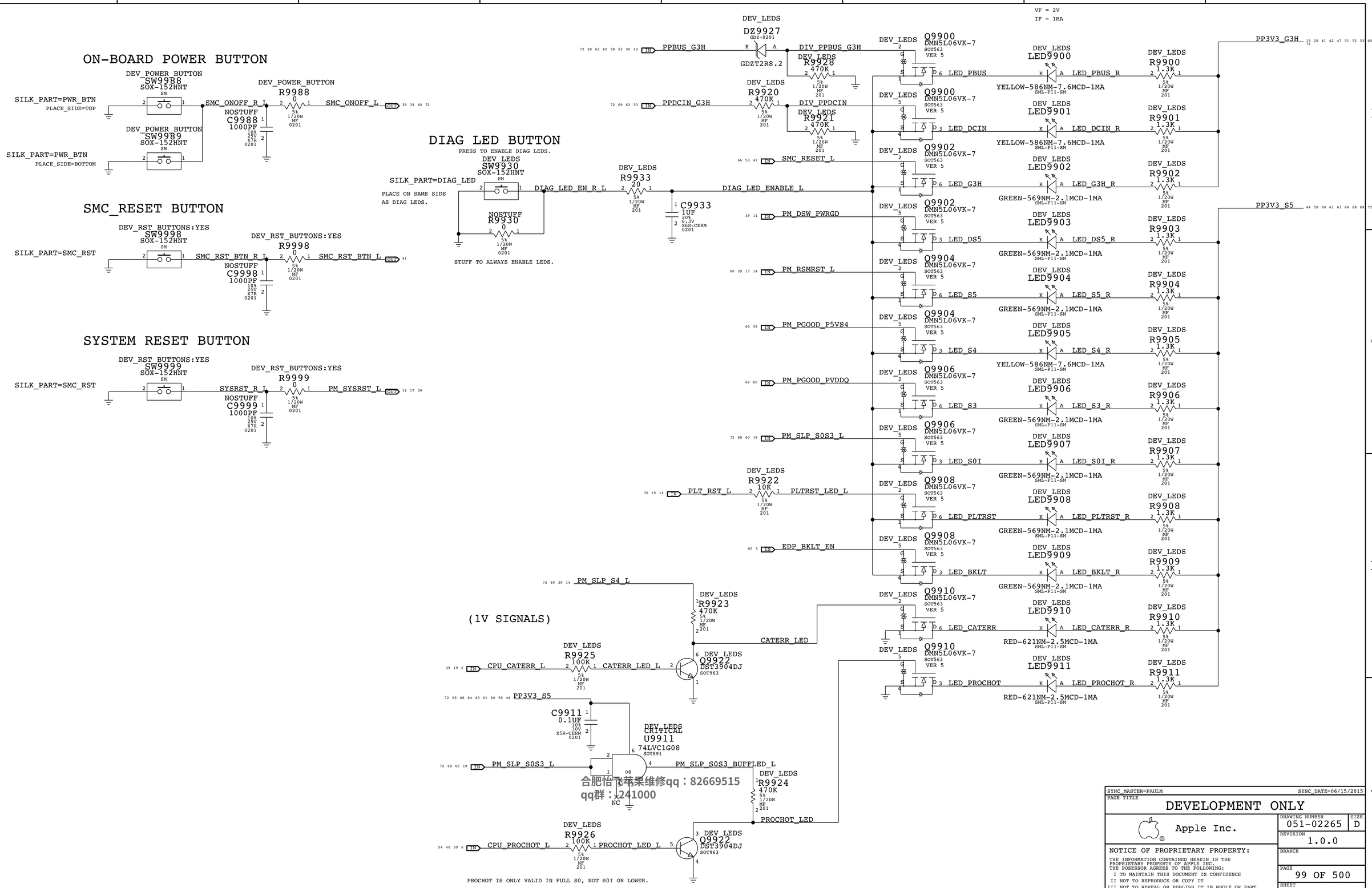

合肥恰飞苹果维修qq：82669515
qq群：241000

52 32 31 =PPBUS_G3H	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
43 =PPDCIN_G3H_SNS	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72
58 =PP5V_S5_LDO	MAKE_BASE=TRUE	PP5V_S5	63 64
66 =PP3V3_G3H_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
40 39 =PP3V3_S5_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
40 =PP3V3_S4_SMC	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
40 =PP3V3_S0_SMC	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
40 =PPVIN_S5_SMCVREF	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
24 23 22 21 =PP1V8_S3_MEM	MAKE_BASE=TRUE	PP1V8_S3	60 63 64
24 23 22 21 =PP1V2_S3_MEM_VDD2	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
24 23 22 21 =PP1V2_S3_MEM_VDDCA	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
24 23 22 21 =PP1V2_S3_MEM_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
20 =PPDDR_S3_MEMVREF	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
25 =PP0V6_S0_MEM_VTT_A	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
25 =PP0V6_S0_MEM_VTT_B	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
20 PPVREF_S3_MEM_VREFDQ_A	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_A	21 22
69 20 PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_A	21 22
20 PPVREF_S3_MEM_VREFDQ_B	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_B	23 24
69 20 PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_B	23 24

CPU RAILS

10 8 =PPVCC_S0_CPU	MAKE_BASE=TRUE	PPVCCCPU_S0G	45 55 63 72
10 8 =PPVCCSA_S0_CPU	MAKE_BASE=TRUE	PPVCCSA_S0G	56 72
11 8 =PPVCCGT_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
11 8 =PPVCCGTX_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
69 10 8 =PP1V2_S3_CPU_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
10 8 =PP1V2_S3_CPU_VDDQC	MAKE_BASE=TRUE	=PP1V2_S3_CPU_VDDQ	8 10 69
10 8 5 =PP0V95_S0_CPU_VCCIO	MAKE_BASE=TRUE	PPVCCIO_S0G	61 63 72
59 54 19 14 10 8 6 =PP1V_S3_CPU_VCCST	MAKE_BASE=TRUE	PP1V_S3	64 69
40 =PP1V_S0_SMC_VCCST			
17 10 8 6 =PP1V_S0SW_CPU_VCCSTG	MAKE_BASE=TRUE	PP1V_S0G	44
10 8 =PP1V_S3_CPU_VCCPLL	MAKE_BASE=TRUE	PP1V_S3	64 69
10 8 =PP1V2_S0SW_CPU_VCCPLLOC	MAKE_BASE=TRUE	PP1V2_S0G	64

PCH RAILS

15 14 12 8 =PP3V_G3H_PCH_VCCRTC	MAKE_BASE=TRUE	PP3V1_RTC	61
14 8 =PP3V3_S5_PCH_VCCDSW	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
16 15 14 13 8 =PP3V3_SUS_PCH_VCCPGPPA	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
19 12 8 =PP3V3_SUS_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 =PP3V3_SUS_PCH_VCCPGPPC	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
8 =PP3V3_SUS_PCH_VCCPGPPD	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 =PP3V3_SUS_PCH_VCCPGPPE	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
8 =PP3V3_SUS_PCH_VCCPGPPG	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 5 =PP3V3_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
47 13 8 =PP3V3_SUS_PCH_VCCSPI	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 =PP3V3_SUS_PCH_VCCRTCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
69 12 8 =PP1V_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 8 =PP1V_SUS_PCH_VCCMPHYAON	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
8 =PP1V_SUS_PCH_VCCCLK1	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 =PP1V_SUS_PCH_VCCCLK2_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
8 =PP1V_SUS_PCH_VCCCLK3	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 =PP1V_SUS_PCH_VCCCLK4_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 =PP1V_SUS_PCH_VCCCLK5_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 8 =PP1V_SUS_PCH_VCCCLK6	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
15 12 =PP1V_SUS_PCH_VCCAPLL	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
14 8 =PP1V8_SUS_PCH_VCCPGPPF	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
12 8 =PP1V8_SUS_PCH_VCCATS	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
12 =PP1V8_SUS_PCH_VCC1P8_SRC	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
12 8 =PPVCCPRIMECORE_SUS_PCH	MAKE_BASE=TRUE	PPVCCPCH_S5G	61 63 72
12 =PP1V_SUSSW_PCH_VCCAMPHYPLL_SRC	MAKE_BASE=TRUE	PP1V_S5GTD	44 69
12 8 =PP1V_SUSSW_PCH_VCCMPHYGT	MAKE_BASE=TRUE	PP1V_S5GTD	44 69
12 8 =PP1V_SUSSW_PCH_VCCSRAM	MAKE_BASE=TRUE	PP1V_S5GTD	44 69
12 8 =PP1V_SUSSW_PCH_VCCAPLLEBB	MAKE_BASE=TRUE	PP1V_S5GTD	44 69
12 =PP1V8_S0_PCH_VCCHDA	MAKE_BASE=TRUE	PP1V8_S0	48 50 51 60 63 64 67 72
18 =PP1V8R1V5_S0_PCH_VCCHDA			
60 19 16 14 13 5 =PP3V3_S0_PCH	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
14 =PP3V3_S4_PCH	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
40 =PP3V3R1V8_S0_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69

SSD RAILS

67 44 PP3V3_S5_SSD	MAKE_BASE=TRUE	PP3V3_S5_SSD_SNS	63
45 =PP3V3_S0_TBT_X_SNS		=PP3V3_TBT_X_S0	27 28

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qq群： 241000

8 CPU_VCCGTXSENSE_P	MAKE_BASE=TRUE	PU_VSNS_CPU_VCCGTX_TP	
8 CPU_VCCGTXSENSE_N	MAKE_BASE=TRUE	PD_VSNS_CPU_VCCGTX_TN	
36 =PP3V3_S0_CAMERA	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
37 =PP5V_S0_ALSCAM	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
66 =PP3V3_S0_LCD	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
66 =PP3V3_S5_LCD	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
66 =PP5V_S0_LCD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
35 =PP3V3_S0_BT_UART	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
35 =PP3V3_S4_BT_UART	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
38 =PP3V3_G3H_KBD	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
38 =PP3V3_S4_KBD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
38 =PP5V_S0_KBD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
34 19 =PP3V3_S4_WLAN	MAKE_BASE=TRUE	PP3V3_S4_WLS	44 63 72
18 =PP3V3_S5_WIRELESS	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
38 =PP3V3_S0_TPAD	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
38 =PP3V3_S4_TPAD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
38 =PP5V_S4_TPAD	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
38 =PPBUS_S4_TPAD	MAKE_BASE=TRUE	PPBUS_G3H_TPAD	43
17 =PP1V_SUS_XDP		=PP1V_SUS_PCH_VCCPRIM	8 12 69
60 17 =PP3V3_SUS_XDP	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
65 =PP5V_S0_BKLT	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
65 =PPVIN_S0SW_LCDBKLTFET	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
38 =PP5V_S0_FAN	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.0850
MIN_LINE_WIDTH=0.3000

USB-C GLOBAL POWER ALIASES

29 =PP3V3_UPC_XA_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XA_LDO	28 29
30 =PP3V3_UPC_XB_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XB_LDO	28 30 63
33 =PP3V3_S5_TBT_X	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
29 =PP5V_XA_USBC	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
30 =PP5V_XB_USBC			
28 =PP5V_USBC			
30 29 =PPHV_EXT_G3H	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 19:33:56 2016

PAGE TITLE
Power Aliases

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DRAWING NUMBER 051-02265 SIZE D
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UNUSED GPIOS, HSIO

Ref	Dir	Net	Property	Property	NC Net
8	IN	VCCPRIM_CORE_VID0	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID0
8	IN	VCCPRIM_CORE_VID1	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID1
16	IN	MLB_DEV_L	MAKE_BASE=TRUE	NO_TEST=1	NC_MLB_DEV_L
16	IN	I2C_UPC_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SDA
16	IN	I2C_UPC_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SCL
13	IN	PCH_BSSB_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_CLK
13	IN	PCH_BSSB_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_DATA
16	IN	TBT_X_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_X_DPMUX_SEL
16	IN	TBT_T_CIO_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CIO_PWR_EN
16	IN	TBT_T_USB_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_USB_PWR_EN
16	IN	TBT_T_PCI_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_PCI_RESET_L
16	IN	TBT_T_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_DPMUX_SEL
15	OUT	=TBT_T_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CLKREQ_L
15	IN	PCIE_CLK100M_TBT_T_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TN
15	IN	PCIE_CLK100M_TBT_T_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TP
15	OUT	PCIE_TBT_T_D2R_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN0
15	OUT	PCIE_TBT_T_D2R_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP0
15	IN	PCIE_TBT_T_R2D_C_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN0
15	IN	PCIE_TBT_T_R2D_C_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP0
15	OUT	PCIE_TBT_T_D2R_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN1
15	OUT	PCIE_TBT_T_D2R_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP1
15	IN	PCIE_TBT_T_R2D_C_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN1
15	IN	PCIE_TBT_T_R2D_C_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP1
15	BI	USB_CAMERA_DFR_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03N
15	BI	USB_CAMERA_DFR_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03P
13	IN	DEBUGUART_SEL_SOC	MAKE_BASE=TRUE	NO_TEST=1	NC_DEBUGUART_SEL_SOC
15	BI	USB3_EXTB_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RN
15	BI	USB3_EXTB_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RP
15	BI	USB3_EXTB_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCN
15	BI	USB3_EXTB_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCP
26	BI	=DP_X_SRC_ML_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CP<3..0>
26	BI	=DP_X_SRC_ML_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CN<3..0>
26	BI	=DP_X_SRC_AUX_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHP
26	BI	=DP_X_SRC_AUX_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHN
15	BI	USB_EXTA_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01N
15	BI	USB_EXTA_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01P

Ref	Dir	Net	Property
15	BI	NC_USB2_05N	NO_TEST=1
15	BI	NC_USB2_05P	NO_TEST=1
15	BI	NC_USB2_06N	NO_TEST=1
15	BI	NC_USB2_06P	NO_TEST=1
15	BI	NC_USB2_07N	NO_TEST=1
15	BI	NC_USB2_07P	NO_TEST=1
15	BI	NC_USB2_09N	NO_TEST=1
15	BI	NC_USB2_09P	NO_TEST=1
15	BI	NC_USB2_10N	NO_TEST=1
15	BI	NC_USB2_10P	NO_TEST=1
30	BI	NC_UPC_XB_I2C_ADDR	NO_TEST=1

GND
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.0850
VOLTAGE=0V

Digital Ground

Ref	Dir	Net	Property	Property	NC Net
16	IN	TP_BT_I2S_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_CLK
16	IN	TP_BT_I2S_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_D2R
16	IN	TP_BT_I2S_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_R2D
16	IN	TP_BT_I2S_SYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_SYNC
36	IN	TP_CAM_GPIO3	MAKE_BASE=TRUE	NO_TEST=1	NC_CAM_GPIO3
6	IN	TP_CPU_AT5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AT5
6	IN	TP_CPU_AU5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AU5
6	IN	TP_CPU_AY4	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AY4
6	IN	TP_CPU_BB3	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB3
6	IN	TP_CPU_BB5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB5
59	IN	TP_CPU_MSM_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_MSM_L
9	IN	TP_CPU_NCTFVSS_A5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A5
9	IN	TP_CPU_NCTFVSS_A70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A70
9	IN	TP_CPU_NCTFVSS_AV1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_AV1
9	IN	TP_CPU_NCTFVSS_B71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_B71
9	IN	TP_CPU_NCTFVSS_BA1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA1
9	IN	TP_CPU_NCTFVSS_BA71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA71
9	IN	TP_CPU_NCTFVSS_BB70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BB70
9	IN	TP_CPU_NCTFVSS_C1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_C1
13	IN	TP_PCH_CLKOUT_LPC1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKOUT_LPC1
14	IN	TP_PCH_GPD7	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPD7
14	IN	TP_PCH_GPP_D0	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D0
16	IN	TP_PCH_GPP_D1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D1
16	IN	TP_PCH_GPP_D3	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D3
16	IN	TP_PCH_GPP_D4	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D4
5	IN	TP_PCH_GPP_E15	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_E15
14	IN	TP_PCH_GPP_F8	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F8
14	IN	TP_PCH_GPP_F9	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F9
14	IN	TP_PCH_GPP_F10	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F10
14	IN	PCH_BT_ROM_BOOT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F11
13	IN	PCH_SOC_DFU_STATUS	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F18
13	IN	SOC_PANIC_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F19
13	IN	SOC_S2R_ACK_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F20
13	IN	SOC_SLEEP_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F21
14	IN	TP_PCH_LANPHYPC	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_LANPHYPC
14	IN	TP_PCH_PME_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_PME_L
14	IN	TP_PCH_SLP_WLAN_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SLP_WLAN_L
13	IN	TP_PCH_STRP_ESPI	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_ESPI
13	IN	TP_PCH_STRP_TLSCONF	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_TLSCONF
60	IN	TP_PMIC_PGC	MAKE_BASE=TRUE	NO_TEST=1	NC_PMIC_PGC
13	IN	TP_SPI_CS1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS1_L
13	IN	TP_SPI_CS2_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS2_L
19	IN	TP_SYSCLK_CLK24M_SSD	MAKE_BASE=TRUE	NO_TEST=1	NC_SYSCLK_CLK24M_SSD
15	IN	TP_USB3_03_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RN
15	IN	TP_USB3_03_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RP
15	IN	TP_USB3_03_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DN
15	IN	TP_USB3_03_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DP
15	IN	TP_USB3_04_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RN
15	IN	TP_USB3_04_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RP
15	IN	TP_USB3_04_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DN
15	IN	TP_USB3_04_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DP
14	IN	PCH_SOC_FORCE_DFU	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_FORCE_DFU
13	OUT	PCH_SOC_WDOG	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_WDOG
14	OUT	UPC_I2C_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_I2C_INT_L
30	IN	TP_UPC_XB_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XB_SWD_DATA
29	IN	TP_UPC_XA_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_DATA
29	IN	TP_UPC_XA_SWD_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_CLK
15	IN	TP_PCIE_CLK100M5P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5P
15	IN	TP_PCIE_CLK100M5N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5N
15	IN	TP_PCH_CLKREQ5_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKREQ5_L
15	IN	TP_ITPXDP_CLK100MP	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MP
15	IN	TP_ITPXDP_CLK100MN	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MN
55	IN	TP_CPUVR_GH1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPUVR_GH1
6	IN	TP_CPU_RSVD_BB69	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB69
6	IN	TP_CPU_RSVD_BB68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB68
6	IN	TP_CPU_RSVD_BA70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA70
6	IN	TP_CPU_RSVD_BA68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA68
6	IN	TP_CPU_RSVD_AW71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW71
6	IN	TP_CPU_RSVD_AW70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW70
6	IN	TP_CPU_RSVD_AK12	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AK12
19	IN	TP_SPKR_ID0	MAKE_BASE=TRUE	NO_TEST=1	NC_SPKR_ID0
60	IN	TP_PGOOD_PVCCIO	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_PVCCIO
60	IN	TP_PGOOD_P1V00	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_P1V00
19	IN	TP_PCH_CLK32K_RTCX2	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK32K_RTCX2
19	IN	TP_PCH_CLK24M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK24M_XTALOUT
19	IN	TP_XDP_BPM_L<3>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<3>
19	IN	TP_XDP_BPM_L<2>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<2>
19	IN	TP_XDP_BPM_L<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<1>

合肥佰飞苹果维修qq：82669515
qq群：241000

Ref	Dir	Net	MAKE_BASE	Net	Dir	Ref
65	BI	=I2C_BKLT_SCL	TRUE	I2C_BKLT_SCL	BI	66 72
65	BI	=I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	BI	66 72

BOM_COST_GROUP=NO COST ITEMS

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LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
NC_ AND NO_TEST SIGNALS

Apple Inc.

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REVISION 1.0.0
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Memory Bit/Byte Swizzle

CPU	MAKE_BASE	DRAM
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MEM_A_DQ<1>	TRUE	=MEM_A_DQ<17>
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MEM_B_DQ<2>	TRUE	=MEM_B_DQ<1>
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qq群： 241000

BOM_COST_GROUP=NO COST ITEMS

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PAGE TITLE
Memory Signal Swaps

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XDP

Pages	Net	Property
17 6	CPU_CFG<3>	FUNC_TEST=TRUE
17 6	ITP_PMODE	FUNC_TEST=TRUE
17 15	XDP_CPU_PRDY_L	FUNC_TEST=TRUE
17 15	XDP_CPU_PREQ_L	FUNC_TEST=TRUE
17	XDP_CPU_PWRBTN_L	FUNC_TEST=TRUE
17 6	XDP_CPU_TCK	FUNC_TEST=TRUE
17 6	XDP_CPU_TDI	FUNC_TEST=TRUE
17 6	XDP_CPU_TDO	FUNC_TEST=TRUE
17 6	XDP_CPU_TMS	FUNC_TEST=TRUE
17 6	XDP_CPU_TRST_L	FUNC_TEST=TRUE
17	XDP_DBRESET_L	FUNC_TEST=TRUE
17 6	XDP_PCH_TCK	FUNC_TEST=TRUE
17 6	XDP_PCH_TDI	FUNC_TEST=TRUE
17 6	XDP_PCH_TDO	FUNC_TEST=TRUE
17 6	XDP_PCH_TMS	FUNC_TEST=TRUE
17 6	XDP_PCH_TRST_L	FUNC_TEST=TRUE
17	XDP_PM_RSMRST_L	FUNC_TEST=TRUE
17	XDP_PRESENT_CPU	FUNC_TEST=TRUE
60 17	XDP_PRESENT_L	FUNC_TEST=TRUE
69 64 63 62 19	PP1V_S5G	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

AUDIO FLEX

Pages	Net	Property
51	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
51	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
51	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
51	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
51	AUD_CONN_RING2	FUNC_TEST=TRUE
51	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
51	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
51	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
51	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
51 48	DMIC1_CLK	FUNC_TEST=TRUE
51 48	DMIC1_DATA	FUNC_TEST=TRUE
51 41	HALL_SENSOR_RIGHT	FUNC_TEST=TRUE
69 67 64 63 60 51 50 48	PP1V8_S0	FUNC_TEST=TRUE
53 52 51 47 42 41 28 19 72 69 68 60	PP3V3_G3H	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

LEFT SPEAKERS

Pages	Net	Property
51 48	8409_SPKR_ID0	FUNC_TEST=TRUE
51 50	SPKRCONN_FL_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_FL_OUT_P	FUNC_TEST=TRUE
51 50	SPKRCONN_RL_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_RL_OUT_P	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

RIGHT SPEAKERS

Pages	Net	Property
51 48	8409_SPKR_ID1	FUNC_TEST=TRUE
51 50	SPKRCONN_FR_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_FR_OUT_P	FUNC_TEST=TRUE
51 50	SPKRCONN_RR_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_RR_OUT_P	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

BATTERY

Pages	Net	Property
52	SYS_DETECT_L	FUNC_TEST=TRUE
72 42	SMBUS_SMC_5_G3H_SCL	FUNC_TEST=TRUE
72 42	SMBUS_SMC_5_G3H_SCL	FUNC_TEST=TRUE

SMC

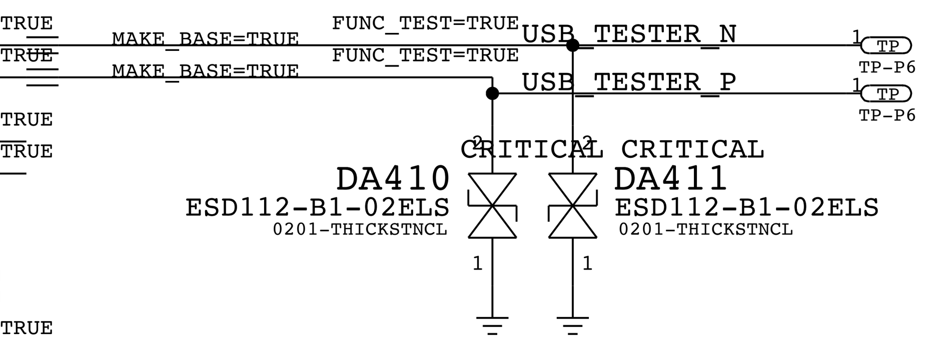
Pages	Net	Property
47 40 39 28	SMC_TCK	FUNC_TEST=TRUE
40 39	SMC_TDI	FUNC_TEST=TRUE
40 39	SMC_TDO	FUNC_TEST=TRUE
47 40 39 28	SMC_TMS	FUNC_TEST=TRUE
41	SMC_DEV_SUPPLY_L	FUNC_TEST=TRUE

BOOTROM

Pages	Net	Property
47 16	SPIROM_USE_MLB	FUNC_TEST=TRUE
47	SPI_MLBROM_CS_L	FUNC_TEST=TRUE
47	SPI_MLB_CLK	FUNC_TEST=TRUE
47	SPI_MLB_CS_L	FUNC_TEST=TRUE
47	SPI_MLB_IO<2>	FUNC_TEST=TRUE
47	SPI_MLB_IO<3>	FUNC_TEST=TRUE
47	SPI_MLB_MISO	FUNC_TEST=TRUE
47	SPI_MLB_MOSI	FUNC_TEST=TRUE

USB2 FIXTURE PORT

Pages	Net	Property
15	TP_USB_TESTERN	FUNC_TEST=TRUE
15	TP_USB_TESTERP	FUNC_TEST=TRUE
69 64 63 60 58 54	PP5V_S4	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE



CAP POWER DISCHARGE

Pages	Net	Property
69 68 63 60 58 53 50 43	PPBUS_G3H	FUNC_TEST=TRUE
69 68 63 53	PPDCIN_G3H	FUNC_TEST=TRUE
53 52	PPDCIN_G3H_CHGR	FUNC_TEST=TRUE
72 66 65	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE

SYSTEM STATE

Pages	Net	Property
68 60 19	PM_SLP_S0S3_L	FUNC_TEST=TRUE
60 39 14	PM_SLP_S0_L	FUNC_TEST=TRUE
66 60 59 39 26 14	PM_SLP_S3_L	FUNC_TEST=TRUE
68 60 39 14	PM_SLP_S4_L	FUNC_TEST=TRUE
60 39 14	PM_SLP_S5_L	FUNC_TEST=TRUE
60 14	PM_SLP_SUS_L	FUNC_TEST=TRUE
41 39 17	PM_PWRBTN_L	FUNC_TEST=TRUE
60 39	ALL_SYS_PWRGD	FUNC_TEST=TRUE

MOJO PORT

Pages	Net	Property
40 39 28	SMC_DEBUGPRT_TX_L	FUNC_TEST=TRUE
40 39 28	SMC_DEBUGPRT_RX_L	FUNC_TEST=TRUE

MISC

Pages	Net	Property
67	SSD_BOOT_CONN_L	FUNC_TEST=TRUE
14	TP_PCH_SLP_A_L	FUNC_TEST=TRUE

CAMERA

Pages	Net	Property
36	CAM_TEST_MODE	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TCK	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TDI	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TDO	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TMS	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TRSTN	FUNC_TEST=TRUE
36	TP_CAM_TEST_MODE0	FUNC_TEST=TRUE
36	TP_CAM_TEST_MODE1	FUNC_TEST=TRUE
36	TP_CAM_TEST_MODE2	FUNC_TEST=TRUE

DISPLAY

Pages	Net	Property
66 5	DP_INT_HPD	FUNC_TEST=TRUE
66 5	EDP_BKLT_PWM	FUNC_TEST=TRUE
66	EDP_INT_AUX_N	FUNC_TEST=TRUE
66	EDP_INT_AUX_P	FUNC_TEST=TRUE
66 5	EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
66	I2C_ALS_SCL_CONN	FUNC_TEST=TRUE
66	I2C_ALS_SDA_CONN	FUNC_TEST=TRUE
70 66	I2C_BKLT_SCL	FUNC_TEST=TRUE
70 66	I2C_BKLT_SDA	FUNC_TEST=TRUE
66	I2C_CAM_SCL_CONN	FUNC_TEST=TRUE
66	I2C_CAM_SDA_CONN	FUNC_TEST=TRUE
66	I2C_TCON_SCL_CONN	FUNC_TEST=TRUE
66	I2C_TCON_SDA_CONN	FUNC_TEST=TRUE
66 16	LCD_IRQ_L	FUNC_TEST=TRUE
66 37	MIPI_CLK_CONN_N	FUNC_TEST=TRUE
66 37	MIPI_CLK_CONN_P	FUNC_TEST=TRUE
66 37	MIPI_DATA_CONN_N	FUNC_TEST=TRUE
66 37	MIPI_DATA_CONN_P	FUNC_TEST=TRUE
66 41	TCON_BKLT_PWM	FUNC_TEST=TRUE
66	PP3V3_S0SW_LCD	FUNC_TEST=TRUE
66	PP5V_S0SW_LCD	FUNC_TEST=TRUE
66 37	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
72 66 65	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

USBC/TBT

Pages	Net	Property
28 26	JTAG_TBT_TCK	FUNC_TEST=TRUE
28 26	JTAG_TBT_TDI	FUNC_TEST=TRUE
28 26	JTAG_TBT_X_TMS	FUNC_TEST=TRUE
26	TBT_X_TEST_EN	FUNC_TEST=TRUE
31 28	PP20V_USBC_XA_VBUS	FUNC_TEST=TRUE
32 28	PP20V_USBC_XB_VBUS	FUNC_TEST=TRUE

POWER

Pages	Net	Property
69 67 64 61 59	PP1V8_S5G	FUNC_TEST=TRUE
59	PP1V_OPC_S0	FUNC_TEST=TRUE
69 63 44	PP3V3_S4_WLS	FUNC_TEST=TRUE
69 68 64 63 61 60 58 44	PP3V3_S5	FUNC_TEST=TRUE
69 64 60	PP3V3_S5G	FUNC_TEST=TRUE
69 63 55 45	PPVCCCPU_S0G	FUNC_TEST=TRUE
69 63 57 45	PPVCCGT_S0G	FUNC_TEST=TRUE
69 63 61	PPVCCIO_S0G	FUNC_TEST=TRUE
59	PPVCCOPC_S0G	FUNC_TEST=TRUE
69 63 61	PPVCCPCH_S5G	FUNC_TEST=TRUE
69 56	PPVCCSA_S0G	FUNC_TEST=TRUE
69 62	PPVTT_S0	FUNC_TEST=TRUE

WIRELESS

Pages	Net	Property
34	JTAG_WLAN_SEL	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TCK	FUNC_TEST=TRUE
34	JTAG_WLAN_TDI	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TDO	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TMS	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TRST	FUNC_TEST=TRUE

TRACKPAD AND KEYBOARD

Pages	Net	Property
39 38	ACT_THERM_TRIP_L	FUNC_TEST=TRUE
38	FAN_LT_PWM	FUNC_TEST=TRUE
38	FAN_LT_TACH	FUNC_TEST=TRUE
38	KBD_BLC_GSLAT	FUNC_TEST=TRUE
38	KBD_BLC_GSSCK	FUNC_TEST=TRUE
38	KBD_BLC_GSSIN	FUNC_TEST=TRUE
38	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
38	KBD_BLC_XBLANK	FUNC_TEST=TRUE
38	KBD_I2C_SCL	FUNC_TEST=TRUE
38	KBD_I2C_SDA	FUNC_TEST=TRUE
38	KBD_INT_L	FUNC_TEST=TRUE
38 16	TPAD_SPI_MOSI	FUNC_TEST=TRUE
38 16	TPAD_SPI_INT_L	FUNC_TEST=TRUE
38	TPAD_SPI_CS_CONN_L	FUNC_TEST=TRUE
38 16	TPAD_SPI_MISO	FUNC_TEST=TRUE
38 16	TPAD_SPI_IF_EN	FUNC_TEST=TRUE
38 16	TPAD_SPI_CLK	FUNC_TEST=TRUE
38	TPAD_VIBE_L	FUNC_TEST=TRUE
41 38	SMC_LSOC_RST	FUNC_TEST=TRUE
68 40 39 38	SMC_ONOFF_L	FUNC_TEST=TRUE
41 40 39	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
68 60 53 52 51 47 42 41 28 19 72 69	PP3V3_G3H	FUNC_TEST=TRUE
69 67 64 63 45 44 43 41	PP3V3_S4	FUNC_TEST=TRUE
69 64 59 57 56 55 54	PP5V_S0	FUNC_TEST=TRUE
38	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
38	PPVIN_S4_TPAD_FUSE	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

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FOR DC/DC

Pages	Net	Property
53	TBA_HPWR_EN_L	FUNC_TEST=TRUE
53	PD_TBA_MPM_DET	FUNC_TEST=TRUE

FOR DEBUG

Pages	Net	Property
29	TP_UPC_XA_DBG_UART_TX	FUNC_TEST=TRUE
29	TP_UPC_XA_DBG_UART_RX	FUNC_TEST=TRUE
30	TP_UPC_XB_DBG_UART_TX	FUNC_TEST=TRUE
30	TP_UPC_XB_DBG_UART_RX	FUNC_TEST=TRUE

NO_TEST nets (column 3)

Pages	Net	Property
66 5	EDP_ML_C_N<0..3>	NO_TEST=1
66 5	EDP_ML_C_P<0..3>	NO_TEST=1
66	EDP_INT_ML_N<0..3>	NO_TEST=1
66	EDP_INT_ML_P<0..3>	NO_TEST=1
35 34	PCIE_AP_D2R_C_N	NO_TEST=1
35 34	PCIE_AP_D2R_C_P	NO_TEST=1
35 15	PCIE_AP_D2R_N	NO_TEST=1
35 15	PCIE_AP_D2R_P	NO_TEST=1
35 15	PCIE_AP_R2D_C_N	NO_TEST=1
35 15	PCIE_AP_R2D_C_P	NO_TEST=1
35 34	PCIE_AP_R2D_N	NO_TEST=1
35 34	PCIE_AP_R2D_P	NO_TEST=1
67 15	PCIE_SSD_D2R_N<0..3>	NO_TEST=1
67 15	PCIE_SSD_D2R_P<0..3>	NO_TEST=1
67 15	PCIE_SSD_R2D_C_N<0..3>	NO_TEST=1
67 15	PCIE_SSD_R2D_C_P<0..3>	NO_TEST=1
67	PCIE_SSD_R2D_N<0..3>	NO_TEST=1
67	PCIE_SSD_R2D_P<0..3>	NO_TEST=1
30	USB_UPC_XB_F_N	NO_TEST=1
30	USB_UPC_XB_F_P	NO_TEST=1
31 26	USBC_XA_D2R_N<1..2>	NO_TEST=1
31 26	USBC_XA_D2R_P<1..2>	NO_TEST=1
31 26	USBC_XA_R2D_C_N<1..2>	NO_TEST=1
31 26	USBC_XA_R2D_C_P<1..2>	NO_TEST=1
31	USBC_XA_R2D_N<1..2>	NO_TEST=1
31	USBC_XA_R2D_P<1..2>	NO_TEST=1
29 28	USBC_XA_USB_BOT_N	NO_TEST=1
29 28	USBC_XA_USB_BOT_P	NO_TEST=1
29 28	USBC_XA_USB_TOP_N	NO_TEST=1
29 28	USBC_XA_USB_TOP_P	NO_TEST=1
32 26	USBC_XB_D2R_N<1..2>	NO_TEST=1
32 26	USBC_XB_D2R_P<1..2>	NO_TEST=1
32 26	USBC_XB_R2D_C_N<1..2>	NO_TEST=1
32 26	USBC_XB_R2D_C_P<1..2>	NO_TEST=1
32	USBC_XB_R2D_N<1..2>	NO_TEST=1
32	USBC_XB_R2D_P<1..2>	NO_TEST=1
32 30	USBC_XB_USB_BOT_N	NO_TEST=1
32 30	USBC_XB_USB_BOT_P	NO_TEST=1
32 30	USBC_XB_USB_TOP_N	NO_TEST=1
32 30	USBC_XB_USB_TOP_P	NO_TEST=1
55	AGND_U7320	NO_TEST=1
	BANJO_VBSTVR1	NO_TEST=1
	BANJO_VBSTVR3	NO_TEST=1
62	BANJO_VBSTVR4	NO_TEST=1
61	BANJO_VBSTVR5	NO_TEST=1
55	CPUVR_BP2	NO_TEST=1
55	CPUVR_PHASE2	
55	CPUVR_SNB1	NO_TEST=1
55	CPUVR_SNB2	NO_TEST=1
59	PD_VSNS_CPU_VCCEOPIO_TN	NO_TEST=1
59	PD_VSNS_CPU_VCCOPC_TN	NO_TEST=1
55	PPVCCCPU_S0G_PH1	NO_TEST=1
55	PPVCCCPU_S0G_PH2	NO_TEST=1
56	PPVCCSA_S0G_R	NO_TEST=1
59	PU_VSNS_CPU_VCCEOPIO_TP	NO_TEST=1
59	PU_VSNS_CPU_VCCOPC_TP	NO_TEST=1
27	VR0V9_IND_TBT_X	NO_TEST=1
12	PP1V_SUS_PCH_VCCAPLL_F	NO_TEST=1
12	PP1V8_S0_PCH_VCCHDA_F	NO_TEST=1

NO_TEST nets (column 1–2)

Pages	Net	Property
25 21 7	MEM_A_CAA<0..9>	NO_TEST=1
25 22 7	MEM_A_CAB<0..9>	NO_TEST=1
25 22 21 7	MEM_A_CKE<0..3>	NO_TEST=1
25 22 21 7	MEM_A_CLK_N<0..1>	NO_TEST=1
25 22 21 7	MEM_A_CLK_P<0..1>	NO_TEST=1
25 22 21 7	MEM_A_CS_L<0..1>	NO_TEST=1
71 7	MEM_A_DQ<0..63>	NO_TEST=1
71 7	MEM_A_DQS_N<0..7>	NO_TEST=1
71 7	MEM_A_DQS_P<0..7>	NO_TEST=1
25 22 21 7	MEM_A_ODT<0>	NO_TEST=1
25 23 7	MEM_B_CAA<0..9>	NO_TEST=1
25 24 7	MEM_B_CAB<0..9>	NO_TEST=1
25 24 23 7	MEM_B_CKE<0..3>	NO_TEST=1
25 24 23 7	MEM_B_CLK_N<0..1>	NO_TEST=1
25 24 23 7	MEM_B_CLK_P<0..1>	NO_TEST=1
25 24 23 7	MEM_B_CS_L<0..1>	NO_TEST=1
71 7	MEM_B_DQ<0..63>	NO_TEST=1
71 7	MEM_B_DQS_N<0..7>	NO_TEST=1
71 7	MEM_B_DQS_P<0..7>	NO_TEST=1
25 24 23 7	MEM_B_ODT<0>	NO_TEST=1
37 36	MEM_CAM_A<0..14>	NO_TEST=1
37 36	MEM_CAM_BA<0..2>	NO_TEST=1
37 36	MEM_CAM_DM<0..1>	NO_TEST=1
37 36	MEM_CAM_DQ<0..15>	NO_TEST=1
37 36	MEM_CAM_DQS_N<0..1>	NO_TEST=1
37 36	MEM_CAM_DQS_P<0..1>	NO_TEST=1
34	RF_0_ANT	NO_TEST=1
34	RF_0_ANT_MATCH_T	NO_TEST=1
34	RF_1_ANT	NO_TEST=1
34	RF_1_ANT_MATCH_T	NO_TEST=1
34	RF_A_0_DIPLEXER	NO_TEST=1
34	RF_A_0_MATCH	NO_TEST=1
34	RF_A_1_DIPLEXER	NO_TEST=1
34	RF_A_1_MATCH	NO_TEST=1
34	RF_G_0_DIPLEXER	NO_TEST=1
34	RF_G_0_MATCH	NO_TEST=1
34	RF_G_1_DIPLEXER	NO_TEST=1
34	RF_G_1_MATCH	NO_TEST=1
55	AGND_U7310	NO_TEST=1
61	BANJO_FBVR2_N	NO_TEST=1
61	BANJO_FBVR2_RC	NO_TEST=1
61	BANJO_SWVR2	NO_TEST=1
61	BANJO_SWVR2_SNUB	NO_TEST=1
61	BANJO_SWVR3R	NO_TEST=1
61	BANJO_SWVR3_SNUB	NO_TEST=1
62	BANJO_VBSTVR1_R	NO_TEST=1
61	BANJO_VBSTVR3_R	NO_TEST=1
62	BANJO_VBSTVR4_R	NO_TEST=1
61	BANJO_VBSTVR5_R	NO_TEST=1
55	CPUVR_BOOT1	NO_TEST=1
55	CPUVR_BP1	NO_TEST=1
55 45	CPUVR_ISNS2_N	NO_TEST=1
55 45	CPUVR_ISNS2_P	NO_TEST=1
55	CPUVR_PHASE1	NO_TEST=1
55	CPUVR_SW1	NO_TEST=1
6	CPU_PROCHOT_R_L	NO_TEST=1
54 8	CPU_VCCGTSENSE_N	NO_TEST=1
14	CPU_VCCST_PWRGD_R	NO_TEST=1
57	GTVR_BP1	
57 45	GTVR_ISNS2_P	NO_TEST=1
57	GTVR_SNB1	NO_TEST=1
57	GTVR_SNB2	NO_TEST=1
57	GTVR_SNB3	NO_TEST=1
57	GTVR_SW1	NO_TEST=1
57	GTVR_SW2	NO_TEST=1
59	P1VOPC_BOOT_RC	NO_TEST=1
59	P1VOPC_DRVH_R	NO_TEST=1
59	P1VOPC_REFIN_R	NO_TEST=1
59	P1VOPC_SNS_R	NO_TEST=1
58	P3V3S5_DRVH_R	NO_TEST=1
58	P5VS4_DRVH_R	NO_TEST=1
56	SAVR_BP	NO_TEST=1
56	SAVR_SNB1	NO_TEST=1
56	SAVR_SW	NO_TEST=1
72 55	VCINP_P5V_U7310	NO_TEST=1
56	AGND_U7470	NO_TEST=1
72 55	VCINP_P5V_U7310	NO_TEST=1
55	VCINP_P5V_U7320	NO_TEST=1
53	TBA_PHASE1	NO_TEST=1
60	PMIC_ENH	NO_TEST=1

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